VSDOpen Conference 2018

# PLACEMENT & ROUTING OF DIGITAL CORE IC TO PADS USING CLOUD BASED EDA TOOL.

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### Design of 6 bit Frequency divider chip using Open source tools

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# ACKNOWLEDGMENTS

- Tim Edwards Open circuit design Magic Tool
- Kunal Ghosh VSD corp :
- Clifford Wolf Yosys Synthesis tool
- Efabless.com

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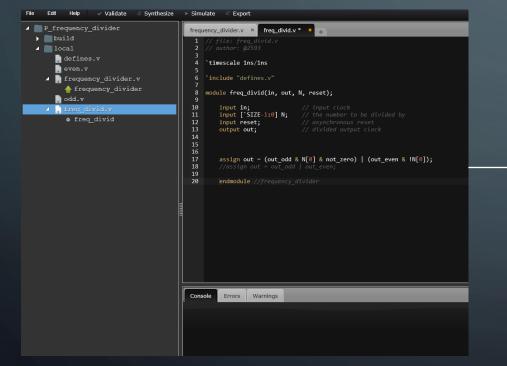
## ABSTRACT

- Process Design flow of Frequency divider chip using open source tools.
- Design of complete chip in Cloud based eda tool.
- Front end tool using CloudV tool.
- Backend design of compiled netlist in OpenGalaxy tool.
- Placement & routing of synthesized core chip to I/O pads followed by addition of substrate and antenna tie down.

## INTEGRATED OPEN SOURCE CLOUD BASED EDA PLATFORM

- Use of one platform consisting of various eda tools embedded into single platform instead of multiple softwares.
- A complete chip can be designed in systematic way from code to layout.
- Errors can be minimised or corrected at every stage interactively.
- Flexible & Robust.
- Works in real time.

### FROM VERILOG CODE TO COMPLETE CHIP



Automated configurable eda tool

Embedded into one platform WWW.VLSISYSTEMDESIGN.COM

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## DIGITAL SYNTHESIS FLOW

Project: frequency_divid	er /home/e	lmioiti/design/P_f	requency_divider	
Checklist				Cleanup Settings
Preparation	Okay	Run	Settings	Purge:
Synthesis	Okay	Run	Settings	
Placement	Okay	Run	Settings	
Static Timing Analysis	Okay	Run	Settings	
Routing	Okay	Run	Settings	
Post-Route STA	Okay	Run	Settings	
Migration	Okay	Run	Settings	
LVS	Okay	Run	Settings	
DRC	Okay	Run	Settings	
Cleanup	Okay	Run	Settings	

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## **REPORTS & SIMULATIONS**

- Synthesis report statistics containing no. of cells , wires inside core chip.
- Placement User can configure the orientation of Pins in Arrange dialog box. Placement of cells are carried out in real time using Simulated annealing algorithm. Graphical view of arrangement is possible here.
- Static timing analysis: timing analysis of each & every flop is obtained and the number of paths analysed is encapsulated in a single report file.
- Routing stage: Uses global routing procedure for connections between cells. User can configure the no.of layers as min or max.
- Post STA: timing analysis is obtained but with improvement in max clock frequency.
- Migration , LVS is carried out & their reports are generated.

#### /home/elmioiti/design/P\_frequency\_divider\_bak/qflow/log/synth.log

3.22.2. Analyzing design hierarchy.. Top module: \frequency\_divider Removed 0 unused modules.

#### 3.23. Printing statistics.

#### === frequency\_divider ===

umber of wires:         184           umber of vire bits:         234           umber of public wires:         184           umber of public wires:         184           umber of memories:         0           umber of menories:         0           umber of cells:         226           AN21X0         5           AN31X0         2           AN32X0         1           AN02X0         3           AN02X0         1           AN02X0         2           AN31X0         2           AND3X0         4           AND4X0         2           AND3X0         4           AND4X0         2           AND3X0         4           DFQX0         1           A021X0         1           A022X0         2           DFFQX0         13           DFFQX0         13           DFFQX0         13           DFRX0X0         6           DFFX0X0         2           MU21X0         8           NA22K0         26           NA31X0         2           NA31X0         2 <td< th=""><th></th><th></th><th></th><th></th></td<>				
umber of public wires:         184           umber of memories:         0           umber of memories:         0           umber of processes:         0           umber of cells:         226           AN21X0         5           AN32X0         1           AN02X0         3           AN03X0         4           AND2X0         2           AN21X0         2           AN32X0         1           AND2X0         3           AND3X0         4           AND2X0         2           A021X0         1           A022X0         2           A032X0         4           DFRQX0         13           DFRQX0         13           DFRQX0         5           E02X0         5           E02X0         5           E02X0         5           E02X0         5           INZ0         2           NA21X0         4           NA21X0         2           NA21X0         2           NA2X0         2           NA2X0         2           NA2X0         2	umber of	wires:	184	
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AN32X0         1           AN02X0         3           AN03X0         4           AN03X0         2           AN05X0         1           A021X0         2           A031X0         2           A032X0         4           DFFQX0         13           DFFQX0         14           MU21X0         6           NA2210         2           M22X0         3           NA211X0         4           NA311X0         4           NA311X0         2           N0311X0         2           N0311X0         2           N0311X0         2           N0311X0         2           N0311X0         2           N0311X0         2           N031X0         7           N04X0         2           ON21X0         3           ON31X0         3           ON21X0	AN21X0		5	
AND2X0         3           AND3X0         4           AND3X0         4           AND4X0         2           AND5X0         1           A021X0         2           A031X0         2           A032X0         4           DFRQX0         13           DFRQX0         6           DFRQX0         5           E02X0         5           NA22X0         3           NA21X0         2           NA311X0         4           NA311X0         2           NO312X0         2           NO312X0         2           NO312X0         2           NO312X0         2           NO312X0         2           ON21X0         2           ON31X0         3           ON2X0         1	AN31X0		2	
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AND4X0         2           AND5X0         1           A0211X0         1           A022X0         2           A031X0         2           A032X0         4           DFFQX0         13           DFFQX0         13           DFRQX0         6           DFFSQX0         2           EN2X0         5           E02X0         5           HVX0         21           MU2IX0         8           NA22X0         3           NA21X0         2           NA31X0         4           NA31X0         2           N031X0         7           N031X0         7           N031X0         2           N031X0         2           N031X0         2           N031X0         2           N031X0         2           N031X0         3           N04X0         2           ON21X0         1	AND2X0		3	
AND5X0         1           A021X0         1           A022X0         2           A031X0         2           A032X0         4           DFFQX0         13           DFRQX0         13           DFRQX0         2           EQ2X0         5           EQ2X0         5           EQ2X0         5           NA21X0         8           NA22X0         3           NA21X0         2           NA21X0         3           NA2X0         26           NA311X0         4           NA31X0         2           N031X0         7           N031X0         7           N031X0         2           ON21X0         2           ON31X0         7           N04X0         2           ON21X0         3           ON21X0         3           ON31X0         3           ON21X0         1	AND3X0		4	
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A0211X0         1           A022X0         2           A031X0         2           A032X0         4           DFFQX0         13           DFRQX0         6           DFRQX0         2           EN2X0         5           ENX0         2           MU21X0         8           NA22X0         3           NA21X0         2           NA31X0         19           N021X0         3           N02X0         7           N031X0         7           N031X0         7           N0421X0         1           N031X0         7           N04X0         2           N031X0         3           ON21X0         3           N04X0         2           ON31X0         3           ON421X0         1	AND5X0		1	
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A031X0         2           A032X0         4           DFFQX0         13           DFFQX0         13           DFRQX0         6           DFRQX0         2           EV2X0         5           EV2X0         5           VIZX0         8           NA22X0         3           NA21X0         2           NA21X0         2           NA31X0         4           NA31X0         19           N021X0         3           N031X0         7           N031X0         7           N031X0         2           OVA2X0         2           OVA2X0         2           OVA31X0         3           OVA2X0         2           OVA31X0         3           OVA2X0         2           OVA2X0         3           OVA2X0         3 </td <td></td> <td></td> <td>2</td> <td></td>			2	
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DFRQX0         6           DFRSQX0         2           EN2X0         5           EQX0         5           IMX0         21           MU2IX0         8           NA221X0         8           NA2200         26           NA311X0         4           NA312X0         2           NA3X0         19           N021X0         2           N0311X0         2           N0312X0         1           N0320         7           N0312X0         1			13	
DFRSQX0         2           EN2X0         5           EQX0         5           INX0         21           MUZIX0         8           NA22X0         3           NA21X0         8           NA21X0         2           NA31X0         2           NA31X0         19           NO21X0         3           N02X0         27           N031X0         7           N031X0         7           N031X0         7           N04X0         2           0A21X0         1           031X0         3           0A21X0         3           0A21X0         1			6	
EN2X0         5           E02X0         5           INX0         21           MU2IX0         8           NA2ZN0         3           NA2IN0         26           NA3IN0         4           NA3IX0         19           NOZIN0         2           N03IX0         2           N03IX0         7           N03X0         7           N03IX0         2           N03IX0         3           042X0         1           N03IX0         3           0041X0         3           0031X0         1			2	
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MU2IX0         8           NA2X0         3           NA2I1X0         8           NA2X0         26           NA3I1X0         4           NA3IX0         2           NA3X0         19           NO2IX0         3           N02X0         27           N03IX0         2           N03IX0         1           N03X0         7           N03IX0         2           0A2IX0         2           0A2IX0         3           0M2IX0         3           0M3IX0         3           0M2IX0         1	E02X0		5	
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NA2I1X0         8           NA2X0         26           NA3I1X0         4           NA3IX0         2           NA3X0         19           N0211X0         3           N02X0         27           N0311X0         2           N0312X0         1           N03X0         7           N04X0         2           OA21X0         15           OH31X0         3           OH21X0         3           OH22K0         1	MU2IX0		8	
NA2X0         26           NA3I1X0         4           NA3I2X0         2           NA3C0         19           N02X1X0         3           N02X0         27           N03I1X0         2           N03I1X0         2           N03IX0         7           N04X0         2           0421X0         15           0131X0         3           042X0         1	NA22X0		3	
NA2X0         26           NA3I1X0         4           NA3I2X0         2           NA3C0         19           N02X1X0         3           N02X0         27           N03I1X0         2           N03I1X0         2           N03IX0         7           N04X0         2           0421X0         15           0131X0         3           042X0         1	NA2I1X0		8	
NA312X0         2           NA3X0         19           N0211X0         3           N02X0         27           N0311X0         2           N0312X0         1           N03X0         7           N04X0         2           OA21X0         15           ON31X0         3           ON2X0         1			26	
NA3X0         19           N0211X0         3           N02X0         27           N0311X0         2           N031X0         1           N03200         7           N04X0         2           0421X0         2           0131X0         3           0021X0         1	NA3I1X0		4	
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N02X0         27           N03I1X0         2           N03I2X0         1           N03X0         7           N04X0         2           0A21X0         2           0N31X0         15           0H31X0         3           0R2X0         1	NA3X0		19	
N0311X0         2           N0312X0         1           N03X0         7           N04X0         2           0A21X0         2           0M21X0         15           0M31X0         3           0M2X0         1	NO2I1X0		3	
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N03X0         7           N04X0         2           0A21X0         2           0N31X0         15           0N31X0         3           0R2X0         1	NO3I1X0		2	
N04X0         2           0A21X0         2           0N21X0         15           0N31X0         3           0R2X0         1	NO3I2X0		1	
0A21X0 2 0N2X00 15 0N3X00 3 0R2X0 1	N03X0		7	
0N21X0 15 0N31X0 3 0R2X0 1	N04X0		2	
0N21X0 15 0N31X0 3 0R2X0 1	0A21X0			
0N31X0 3 0R2X0 1			15	
0R2X0 1				
	OR5X0			

3.24. Executing CHECK pass (checking for obvious problems). checking module frequency\_divider.. found and reported 0 problems.

4. Executing DFFLIBMAP pass (mapping DFF cells to sequential cells from liberty file). cell DFFQX0 (noninv, pins=3, area=49.19) is a direct match for cell type § DFF N. cell OFK0X0 (noninv, pins=3, area=49.19) is a direct match for cell type § DFF P.

### Synthesis reports:

Running yosys for verilog parsing and synthesis yosys -s frequency\_divider.ys

yosys -- Yosys Open SYnthesis Suite

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/----/

Yosys 0.6+138 (git shal 7cddab0, gcc 4.7.4 -fPIC -Os)

-- Executing script file `frequency\_divider.ys' --

Executing Liberty frontend.
 Imported 923 cell types from liberty file.

2. Executing Verilog-2005 frontend. Parsing Verilog input from `/home/elmioiti/design/P\_frequency\_divider/qflow/source/frequency\_divider.v' to AST representation. Generating RTLIL representation for module `\frequency\_divider'. Successfully finished Verilog frontend.

3. Executing SYNTH pass.

3.1. Executing HIERARCHY pass (managing design hierarchy).

3.1.1. Analyzing design hierarchy.. Top module: \frequency\_divider

3.1.2. Analyzing design hierarchy.. Top module: \frequency\_divider

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### Config of orientation of I/O pins at core cell

G placment and routing of wires 🕸 efabless - Toolbox	<i>e</i> OpenGalaxy   efabless	× 📑					
<b>4</b>							
Open Galaxy Proje	ct Manager	↑ _ □ X			(	Qflow Manager	↑ _ □ ×
User: anand301003	Settings Help	Quit	User: anand301003				
- Sector - S			Project: P_freque	ncy_divider_bak	/home/elmic	oiti/design/P_frequency_div	vider_bak
Projects (/home/elmioiti/design/)			Checklist	1			Placement Settings
Available Projects:	PDK	· · · · · · · · · · · · · · · · · · ·	Preparation	Okav	Run	Settings	Initial density: 1.0
DEMO_LS_3VX2 /home/elmioiti/des	ign/DEMO_LS_3VX XFAB : EFXH		ricparation				Aspect ratio: 1.0
P_frequency_divider /home/elmioiti/des	Transfer State Sta		Synthesis	Okay	Run	n Settings	Create power stripes: 💌
P_frequency_divider_bak /home/elmioiti/des		i Galaxy Qflow Pin I	AND A DESCRIPTION OF A DESCRIPTION		- 🗆 🗙	Settings	Stripe width: 2.0
P_raven /home/elmioiti/des P_raven_spi /home/elmioiti/des	N_vector Top: Right: Right: Bott	tom: 🗆 Left: 🛪 P	ermute: 💌 Start %:	0 Stop %: 100			Stripe pitch: 50.0
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				Preparation	Okay	Run	Settings	Initial density: 1.0 Aspect ratio: 1.0
B			PDK	Synthesis	Okay	Run	Settings	Create power stripes: 🗙
			XFAB : EFXH018A XFAB : EFXH018C	Placement	In progress	Stop	Settings	Stripe width: 2.0 Stripe pitch: 50.0
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			XFAB : EFXH018C XFAB : EFXH018C	Routing	(not done)	Run	Settings	Arrange Pin
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				Migration	(not done)	Run	Settings	
			elete	LVS	(not done)	Run	Settings	
			thesis Flow Pad Frame	DRC	(not done)	Rurie	Settings	
			+	Cleanup	(not done)	Run	Settings	
MSG>			son	Preparing pin placement Running GrayWolf placeme grayWolf frequency_divi	nt	equency_divider.ce	12	
MSG> Synthesize design P_frequ	ency_divider_bak (/home/	elmioiti/design/P_tre	equency_divider_bak)	Close	əlp			

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### **RESULTS AND WIP**

/16.8 ps

34 4 : NA22X0 3/Q -> DFFQX4 5/D

Jesign meets minimum hold timing.

Number of paths analyzed: 77

Top 20 maximu	m delay paths:		
Path input pi	n N[1] to DFRRQX4	6/D delay 133	3.45 ps
0.0 ps	N[1]:	->	OR5X4 1/E
589.7 ps	even 0 not zero:	OR5X4 1/Q ->	AND2X4_1/A
795.1 ps	enable_odd:	AND2X4_1/Q ->	INX1_2/A
1038.0 ps	128 :	INX1 2/Q ->	N02X1 4/B
1228.2 ps	145 :	NO2X1 4/Q ->	AN32X1 1/C
1462.5 ps	39 :	AN32X1 1/Q ->	DFRRQX4 6/D
		ta de la constante de la calega de la constante de la constante de la constante de la constante de la constante Constante de la constante de la	and the second second second

Path input pin N[1] to DFRQX4\_7/D delay 1284.38 ps

0.0 ps	N[1]:		->	OR5X4_1/E
589.7 ps	even_0_not_zero:	OR5X4_1/Q	->	AND2X4_1/A
795.1 ps	enable_odd:	AND2X4_1/Q	->	INX1_2/A
1038.0 ps	128 :	INX1 2/Q	->	N02X2 6/A
1296.6 ps	_99_:	N02X2_6/Q	->	0A21X0_1/B
1817.5 ps	100 :	0A21X0 1/Q	->	A0211X0_1/C
2528.6 ps	_350_:	A0211X0_1/Q	->	DFRQX4_7/D

Path input pin N[1] to DFFQX4\_13/D delay 1193.4 ps

### STA REPORT

Design meets minimum hold timing

No.of paths analysed: 77

Max path delay : N[1] to DFRRQX4\_6/D is 1333.45 ps

Min path delay : DFRRQX4\_5/C to DFRRQX4\_5/D is 632.357ps

low terminated normally with no errors and 0 warning[s]

unning getfillcell to determine cell to use for fill. etfillcell.tcl frequency\_divider /ef/tech/XFAB.3/EFXH018C/libs.ref/lef/D\_CELLS/xh018\_D\_CELLS.lef DECAP Ising cell DECAP for fill Running place2def to translate graywolf output to DEF format lace2def.tcl frequency\_divider DECAP Running place2def.tcl DEF database: nanometers imits: xbot = -360.5 ybot = -136 xtop = 8298.5 ytop = 6696 Core values: 31.5 0 8347.5 6832 Offsets: 31.5 0 5 routing layers 113 horizontal tracks from -61.0 to 6832.0 step 61.0 (M1, M3, ...) 138 vertical tracks from -189.0 to 8505.0 step 63.0 (M2, M4, ...) Done with place2def.tcl Nunning addspacers to generate power stripes and align cell right edge addspacers.tcl -techlef /ef/tech/XFAB.3/EFXH018C/libs.ref/techLEF/xh018\_xx51\_MET5\_METMID.lef -stripe 2.0 50. /ef/tech/XFAB.3/EFXH018C/libs.ref/lef/D\_CELLS/xh018\_D\_CELLS.lef DECAP Reading technology LEF file /ef/tech/XFAB.3/EFXH018C/libs.ref/techLEF/xh018\_xx51\_MET5\_METMID.lef. Reading DECAP macros from LEF file. Reading DEF file frequency\_divider.def. . . lumber of rows is 14 ongest row has width 83.475 um addspacers: No room for stripes, pitch reduced from 49770.0 to 34902.0. addspacers: Inserting 2 stripes of width 1.89 um (2.0 um requested) Pitch 34.902 um, offset 23.94 um stretch: Number of components is 264 Analysis of DEF file: Number of components = 236 New number of components = 264 Number of rows = 14 Stripe width 1890 fits 3 VIA1\_X\_so at cut width 260.0 separation 260.0 Stripe width 1890 fits 3 VIA2\_so at cut width 260.0 separation 260.0 Stripe width 1890 fits 3 VIA3\_so at cut width 260.0 separation 260.0 Stripe width 1890 fits 3 VIA4 so at cut width 260.0 separation 260.0 width 1800 fite 2 VIATE X co at cut width 360 0 constation 350

### PLACEMENT REPORT

	User input	Practical output
Stripe width	2 µm	1.89 µm
Stripe pitch	50 µm	34.902 µm

		/home/elmioiti/design/P_frequency_divider_bak/qflow/log/sta.log
	Open Galaxy Text Report	
	/home/elmioiti/design/P_frequency_divider_bak/qflow/log/sta.log	0.0 ps in_bF_buf2: BUX2_7/Q -> DFFQX4_2/CN
		618.2 ps odd_0_counter2_1_: DFFQX4_2/Q -> ON21X0_5/B
STA log	Qflow static timing analysis logfile created on Sat Aug 4 04:23:37 PDT 2018	886.9 ps66_: ON21X0_5/Q -> NO211X0_1/AN
	Running vesta static timing analysis	1185.6 ps67_: N02I1X0_1/Q -> NA2X0_14/B
() ()	<pre>vestalong frequency_divider.rtlnopwr.v /ef/tech/XFAB.3/EFXH018C/libs.ref/liberty/D_CELLS/D_CELLS_LPM05_typ_1_80V_25C.lib</pre>	1424.1 ps69_: NA2X0_14/Q -> MU2IX1_6/IN1
$   \setminus d$ file		1651.3 ps70_: MU2IX1_6/Q -> MU2IX1_7/IN1
	Vesta static timing analysis tool	1850.2 ps342_: MU2IX1_7/Q -> DFFQX4_3/D
	(c) 2013-2017 Tim Edwards, Open Circuit Design	
	A	Computed maximum clock frequency (zero slack) = 464.135 MHz
	Parsing library "D_CELLS_LPMOS_typ_1_80V_25C"	
$\Pi \Lambda U$	End of library at line 426120	Number of paths analyzed: 29
	Parsing module "frequency_divider"	NUMBERS GARANGEREN AREAS SANSTEREN AREAS SANSTER
	Lib Read: Processed 426121 lines.	Top 20 minimum delay paths:
Design meets minimum hold timing.	Verilog netlist read: Processed 240 lines.	Path DFRRQX4_5/C to DFRRQX4_5/D delay 632.357 ps
	Number of paths analyzed: 29	0.0 ps in bF buf0: BUX2 9/Q -> DFRRQX4 5/C
	The 20 environs delay patho	479.7 ps even 0 counter 5 : DFRRQX4 5/Q -> AN31X1 1/D
Number of paths analyzed: 77	Top 20 maximum delay paths:	543.8 ps 31 : AN31X1 1/Q -> NO2X0 3/A
Tumber of parts anacyzed. "	Path DFF0X4_9/CN to DFF0X4_12/D delay 2154.55 ps	606.1 ps NO2X0_3/Q -> DFRRQX4_5/D
Top 20 maximum delay paths:	0.0 ps in bF buf4: BUX2 5/0 -> DFFQX4 9/CN	
Path input pin N[1] to DFRRQX4 6/D delay 1333.45 ps	603.9 ps odd_0_initial_begin_1: DFFQX4_9/Q -> N02X1_6/B	Path DFRSQX4 1/C to DFRSQX4 1/D delay 667.499 ps
	797.5 ps161_: N02X1_6/Q -> NA2X2_1/A	
0.0 ps N[1]: -> 0R5X4_1/E	984.4 ps162_: NA2X2_1/Q -> OII31X0_2/C	그는 것 같은 것 같
589.7 ps even_0_not_zero: OR5X4_1/Q -> AND2X4_1/A	1314.4 ps46 : 0N31X0_2/Q -> NA2X0_12/A 1566.0 ps49 : NA2X0_12/Q -> A032X1_3/E	399.2 ps even_0_counter_0: DFRSQX4_1/Q -> NA2I1X0_2/B
795.1 ps enable_odd: AND2X4_1/Q -> INX1_2/A		488.0 ps13_: NA2I1X0_2/Q -> NA3X0_3/B
1038.0 ps128_: INX1_2/Q -> N02X1_4/B	1973.9 ps364_: A032X1_3/Q -> DFFQX4_12/D	608.7 ps _2_0: NA3X0_3/Q -> DFRSQX4_1/D
1228.2 ps145_: N02X1_4/Q -> AN32X1_1/C	noth DECOVA 11/CH to DECOVA 12/D dolaw 1011 27 pr	
1462.5 ps	Path DFF0X4_11/CN to DFF0X4_13/D delay 1911.27 ps	Path DFRSQX4_2/C to DFRSQX4_2/D delay 704.881 ps
	0.0 ps in_bF_buf1: BUX2_8/Q -> DFFQX4_11/CN 614.2 ps odd 0 initial begin 3 : DFFQX4_11/Q -> N03X4_1/B	0.0 ps in_bF_buf0: BUX2_9/Q -> DFRSQX4_2/C
Path input pin N[1] to DFRQX4_7/D delay 1284.38 ps	861.3 ps 149 : NO3X4 1/Q -> ND3X4 1/A	356.5 ps even_0_out_counter: DFRSQX4_2/Q -> ON31X0_1/D
0.0 ps N[1]: -> OR5X4_1/E	1137.0 ps 155 : ANO3X4 1/Q -> N02X2 3/A	469.5 ps ON31X0_1/Q -> NA2X0_2/A
589.7 ps even_0_not_zero: OR5X4_1/Q -> AND2X4_1/A	$137.0 \text{ ps}$ $1352.5 \text{ ps}$ $1362.1 \text{ NO2X2} 3/\text{Q} \rightarrow \text{NO2X2} 3/\text{Q}$	558.8 ps3_: NA2X0_2/Q -> DFRSQX4_2/D
795.1 ps enable odd: AND2X4 1/Q -> INX1 2/A	1823.8 ps 36_5 : A031X0 1/Q -> DFFQX4_13/D	
1038.0 ps 128 : INX1 2/Q -> NO2X2 6/A	1023.0 h2 M017/0_1/d -> 0.L.dv4_19/0	Path DFRQX4_4/C to DFRRQX4_6/D delay 720.64 ps
1296.6 ps 99 : N02X2 6/Q -> 0A21X0 1/B	Path DFFQX4_11/CN to DFFQX4_5/D delay 1827.87 ps	0.0 ps in bF buf3: BUX2 6/Q -> DFRQX4 4/C
1817.5 ps 100 : 0A21X0_1/Q -> A0211X0_1/C	0.0 ps in bF buf1: BUX2 8/Q -> DFFQX4 11/CN	369.7 ps odd 0 old N 3 : DFRQX4 4/Q -> NO2X2 2/B
2528.6 ps A0211X0_1/Q -> DFRQX4_7/D	614.2 ps odd 0 initial begin 3 : DFFQX4 11/Q -> N03X4 1/B	438.8 ps 136 : N02X2 2/Q -> N03I1X2 2/B
	861.3 ps 149 NO3X4 1/Q -> AND5X4 1/B	504.6 ps 139 : N0311X2 2/Q -> AW32X1 1/B
Path input pin N[1] to DFFQX4 13/D delay 1193.4 ps	1350.3 ps 83 : AND5X4 1/Q -> ON21X0 7/A	624.2 ps 39 : AN32X1 1/Q -> DFRQX4 6/D
Fach input bin will to predva_is/b decay iiss.4 bs	1570.1 ps 87 : ON21X0 7/Q -> NA22X0 3/B	024,2 ps
	1889.4 ps34 4 : NA22X0 3/Q -> DFFQX4 5/D	Dath DEDOVA D/C to DEDOVA D/D dolay 730 154 pc
		Path DFRQX4_9/C to DFRQX4_9/D delay 730.154 ps
Ť de la constante de	Path DFFQX4 2/CN to DFFQX4 6/D delay 1807.52 ps	0.0 ps in bF buf3: $BUX2_6/Q \rightarrow DFRQX4_9/C$
	0.0 ps in_bF_buf2: BUX2_7/Q -> DFFQX4_2/CN	460.9 ps odd_0_counter_2_: DFRQX4_9/Q -> N02X2_7/B
	618.2 ps odd 0 counter2 1 : DFFQX4 2/Q -> N02X1 9/B	558.7 ps107_: N02X2_7/Q -> N03X2_2/C
	809.2 ps 77 : NO2X1 9/Q -> NA3X0 11/C	634.5 ps109_: NO3X2_2/Q -> MU2IX1_8/IN1
	1072.4 ps 90 : NA3XO 11/Q -> ON21XO 8/B	721.7 ps352_: MU2IX1_8/Q -> DFRQX4_9/D
	1392.5 ps 91 : ON21X0 8/Q -> A032X1 4/C	
$  \langle \cap \rangle$	1878.1 ps 34_5 : A032X1 4/Q -> DFFQX4 6/D	Path DFFQX4_11/CN to DFFQX4_11/D delay 749.951 ps
		0.0 ps in_bF_buf1; BUX2_8/Q -> DFFQX4_11/CN
	Path DFFQX4_11/CN to DFFQX4_4/D delay 1789.11 ps	397.7 ps odd_0_initial_begin_3_: DFFQX4_11/Q -> NO3X2_1/B
	0.0 ps in bF buf1: BUX2 8/Q -> DFFQX4 11/CN	482.1 ps40_: N03X2 1/Q -> ON21X0_3/B
	614.2 ps odd_0_initial_begin_3 : DFFQX4_11/Q -> NO3X4_1/B	584.0 ps 42 : ON21X0 3/Q -> NA2X0 11/B
$1/1 \land$	861.3 ps 149: N03X4 1/0 -> NA3X2 1/A	662.7 ps 36 3 : NA2X0 11/Q -> DFFQX4 11/D
$   / \bigcirc$		
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		12/24/2016 13

### ROUTING STAGE

User: anand301003

Help

Quit

Settings

1.1 🗐 🗖 grouter 🗖 Open Galaxy Project M... 🔲 Qflow Manager

	Qf	low Manager		↑ _ □ X
User: anand301003				
Project: P_frequency_	divider_bak /	home/elmioiti/desię	gn/P_frequency	/_divider_bak
Checklist				Route Settings
Preparation	Okay	Run	Settings	Show graphic view: × - Route layers: max
Synthesis	Okay	Run	Settings	Houte layers. Inax
Placement	Okay	Run	Settings	
Static Timing Analysis	Okay	Run	Settings	
Routing	In progress	Stop	Settings	
Post-Route STA	(not done)	Run	Settings	
Migration	(not done)	Run	Settings	
LVS	(not done)	Run	Settings	
DRC	(not done)	Run	Settings	
Cleanup	(not done)	Run	Settings	
Running qrouter 1.4.19.T grouter -noc -s frequen ls: No match.	cy_divider.cfg			
Close	əlp			

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### Routing reports

TimberWolfSC version:v6.0 date:Mon May 25 21:19:07 EDT 1992 Row-Based Placement and Global Routing Program Authors: Carl Sechen, Kai-Win Lee, and Bill Swartz, Yale University 0

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 20 21 22 23 24 25 26 27 16 17 18 19 28 29 30 35 36 37 38 39 40 41 42 43 31 32 33 34 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100 101 102 103 104 105 106 107 108 109 110 111 112 113 114 115 116 117 118 119 120 121 122 123 124 125 126 127 128 129 130 131 132 133 134 135 136 137 138 139 140 141 142 143 144 145 146 147 148 149 150 151 152 153 154 155 156 157 158 block left edge is at -185 the longest block length is 8694 building the steiner trees rebuilding the steiner tree

----start doing coarse global routing -----ITERATION 1

longest Row is:1 Its length is:8316 doing feed-through pins assignment building the net-tree now ! set up the global routing grids the starting value of tracks = 95 tracks = 87 at attempts = 1000 tracks = 86 at attempts = 2000 tracks = 86 at attempts = 3000 tracks = 86 at attempts = 4000 tracks = 86 at attempts = 5000 tracks = 86 at attempts = 6000 removing redundant feed-through pins the connectivity of all the nets is verified

block left edge is at -185 the longest block length is 8694 building the steiner trees rebuilding the steiner tree syntax version:v1.1 date:Mon May 25 21:11:10 EDT 1992 TimberWolf System Syntax Checker Authors: Carl Sechen, Kai-Win Lee, Bill Swartz, Dahe Chen, and Jimmy Lam Yale University

Read 50 objects so far... Read 100 objects so far... Read 150 objects so far... Read 200 objects so far... No syntax errors were found

syntax terminated normally with no errors and 0 warning[s]

Total stdcells :236 Total cell width :1.16e+05 Total cell height :1.15e+05 Total cell area :5.65e+07 Total core area :5.65e+07 Average cell height:4.88e+02

nocut - replacement for Mincut version:v[î.0 date:Mon May 25 21:09:40 EDT 1992 TimberWolf System Floorplan Setup Program Authors: Carl Sechen, Bill Swartz, Yale University

Read 50 objects so far... Read 100 objects so far... Read 150 objects so far... Read 200 objects so far... Splitting frequency\_divider.cel into frequency\_divider.scel and frequency\_divider.mcel... done!

nocut - replacement for Mincut terminated normally with no errors and 0 warning[s]

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## **RESULTS AND WIP**

200 objects so tar... syntax errors were found

syntax terminated normally with no errors and 0 warning[s]

Total stdcells	:236
Total cell width	:1.16e+05
Total cell height	:1.15e+05
Total cell area	:5.65e+07
Total core area	:5.65e+07

nocut - replacement for Mincut version:v[.0 date:Mon May 25 21:09:40 EDT 1992 TimberWolf System Floorplan Setup Program Authors: Carl Sechen, Bill Swartz, Yale University

Read 50 objects so far...

4	
Total stdcells	:314
Total cell width	:1.52e+05
Total cell height	:1.53e+05
Total cell area	:7.42e+07
Total core area	:7.42e+07
Average cell heigh	t:4.88e+02

attributes	N=6	N=8
Total stdcells	236	314
Total cell width	116000 nm	152000 nm
Total cell height	115000 nm	153000 nm
Total cell area	56500 μm	74200 µm
Total core area	56500 µm	74200 µm
Average cell height Horizontal tracks Vertical tracks No. of Routing layers	488 μm 113 138	488 μm 137 147
No. of Routing layers	6	6

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# Routing reports cont'd

----start doing coarse global routing -----ITERATION 1

longest Row is:1 Its length is:8316 doing feed-through pins assignment building the net-tree now ! set up the global routing grids the starting value of tracks = 98 tracks = 85 at attempts = 1000 tracks = 85 at attempts = 2000 tracks = 85 at attempts = 3000 tracks = 85 at attempts = 4000 tracks = 85 at attempts = 5000 tracks = 85 at attempts = 5000 tracks = 85 at attempts = 6000 removing redundant feed-through pins the connectivity of all the nets is verified

block left edge is at -185 the longest block length is 8694 building the steiner trees rebuilding the steiner tree

----start doing coarse global routing -----ITERATION 1

longest Row is:1 Its length is:8316 doing feed-through pins assignment building the net-tree now ! set up the global routing grids the starting value of tracks = 111 tracks = 109 at attempts = 1000 tracks = 109 at attempts = 2000 tracks = 109 at attempts = 3000 tracks = 109 at attempts = 4000 tracks = 109 at attempts = 5000 tracks = 109 at attempts = 6000 removing redundant feed-through pins the connectivity of all the nets is verified

Finished routing net 104 Nets remaining: 47 Finished routing net 106 Nets remaining: 46 Finished routing net 109 Nets remaining: 45 Finished routing net 35 <2> Nets remaining: 44 Finished routing net 110 Nets remaining: 43 Finished routing net 112 Nets remaining: 42 Finished routing net 113 Nets remaining: 41 Finished routing net 35 <3> Nets remaining: 40 Finished routing net 114 Nets remaining: 39 Finished routing net 116 Nets remaining: 38 Finished routing net 117 Nets remaining: 37 Finished routing net 118 Nets remaining: 36 Finished routing net 35 <4> Nets remaining: 35 Finished routing net 119 Nets remaining: 34 Finished routing net 120 Nets remaining: 33 Finished routing net 121 Nets remaining: 32 Finished routing net 122 Nets remaining: 31 Finished routing net 123 Nets remaining: 30 Finished routing net 124 Nets remaining: 29 Finished routing net 35 <5> Nets remaining: 28 Finished routing net 125 Nets remaining: 27 Finished routing net 126 Nets remaining: 26 Finished routing net 37 Nets remaining: 25 Finished routing net 127 Nets remaining: 24 Finished routing net 38 Nets remaining: 23 Finished routing net 108 Nets remaining: 22 Finished routing net out Nets remaining: 21

Progress: Stage 1 total routes completed: 550 Failed net routes: 20 \*\*\* Running stage2 routing with options mask 10, effort 10 Nets remaining: 20 Nets remaining: 19 Best route of \_76\_ collides with net: \_75\_

Progress: Stage 1 total routes completed: 550 Failed net routes: 20 ..... \*\*\* Running stage2 routing with options mask 10, effort 10 Nets remaining: 20 Nets remaining: 19 Best route of 76 collides with net: 75 Ripping up blocking net 75 Nets remaining: 19 Best route of 34 <2> collides with net: N<2> Ripping up blocking net N<2> Nets remaining: 19 Nets remaining: 18 Nets remaining: 17 Best route of 54 collides with nets: 48 N<4> Ripping up blocking net 48 Ripping up blocking net N<4> Nets remaining: 18 Nets remaining: 17 Nets remaining: 16 Best route of 142 collides with net: 141 Ripping up blocking net 141 Nets remaining: 16 Best route of 31\_ collides with nets: \_27\_ \_2\_<5> Ripping up blocking net \_27\_ Ripping up blocking net \_2\_<5> Nets remaining: 17 Nets remaining: 16 Nets remaining: 15 Best route of 95 collides with net: 92 Ripping up blocking net 92 Nets remaining: 15 Best route of odd 0.counter2<4> collides with net: odd 0.counter2<1> Ripping up blocking net odd 0.counter2<1> Nets remaining: 15 Best route of \_149\_ collides with net: \_148\_ Ripping up blocking net 148 Nets remaining: 15 Best route of even 0.counter<4> collides with net: even 0.counter<2> Ripping up blocking net even\_0.counter<2> Nets remaining: 15 Best route of N<3> collides with net: N<0> Ripping up blocking net N<O> Nets remaining: 15 Nets remaining: 14 Nets remaining: 13 Nets remaining: 12 Best route of \_75\_ collides with net: in Ripping up blocking net in Nets remaining: 12 Nets remaining: 11 Nets remaining: 10 Nets remaining: 9 Nets remaining: 8 Nets remaining: 7 Best route of 2 <5> collides with net: 84 Ripping up blocking net 84 Nets remaining: 7 Nets remaining: 6 Nets remaining: 5 Nets remaining: 4

### 2<sup>nd</sup> Stage of Routing: No failed routes

..... Progress: Stage 2 total routes completed: 637 No failed routes! \*\*\* Running stage3 routing with defaults, 1st round Finished routing net N<O> Nets remaining: 245 Finished routing net N<1> Nets remaining: 244 Finished routing net N<4> Nets remaining: 243 Finished routing net N<5> Nets remaining: 242 Finished routing net N<2> Nets remaining: 241 Failed to remove stacked via at grid point 56 66. Failed to route net in bF\$buf4; restoring original Finished routing net in bF\$buf3 Nets remaining: 239 Finished routing net in bF\$buf2 Nets remaining: 238 Finished routing net in bF\$buf1 Nets remaining: 237 Finished routing net in\_bF\$buf0 Nets remaining: 236 Finished routing net N<3> Nets remaining: 235 Finished routing net enable even Nets remaining: 234 Finished routing net enable odd Nets remaining: 233 Finished routing net \_9\_ Nets remaining: 232 Finished routing net \_24\_ Nets remaining: 231 Finished routing net 155 Nets remaining: 230 Finished routing net odd 0.counter2<0> Nets remaining: 229 Finished routing net even 0.counter<2> Nets remaining: 228 Finished routing net even 0.counter<0> Nets remaining: 227 Finished routing net 10 Nets remaining: 226 Finished routing net 17 Nets remaining: 225 Finished routing net \_128\_ Nets remaining: 224 Finished routing net 152 Nets remaining: 223

TimberWolfSC terminated normally with no errors and 0 warning[s]

twflow terminated normally with no errors and 0 warning[s]

Running getfillcell to determine cell to use for fill. getfillcell.tcl frequency divider /ef/tech/XFAB.3/EFXH018C/libs.ref/lef/D CELLS/xh018 D CELLS.lef DECAP Jsing cell DECAP for fill Running place2def to translate graywolf output to DEF format. place2def.tcl frequency divider DECAP Running place2def.tcl DEF database: nanometers \_imits: xbot = -360.5 ybot = -136 xtop = 8298.5 ytop = 6696 Core values: 31.5 0 8347.5 6832 Offsets: 31.5 0 6 routing layers 113 horizontal tracks from -61.0 to 6832.0 step 61.0 (M1, M3, ...) 138 vertical tracks from -189.0 to 8505.0 step 63.0 (M2, M4, ...) Done with place2def.tcl Running addspacers to generate power stripes and align cell right edge addspacers.tcl -techlef /ef/tech/XFAB.3/EFXH018C/libs.ref/techLEF/xh018 xx51 MET5 METMID.lef -stripe 2.0 50. /ef/tech/XFAB.3/EFXH018C/libs.ref/lef/D CELLS/xh018 D CELLS.lef DECAP Reading technology LEF file /ef/tech/XFAB.3/EFXH018C/libs.ref/techLEF/xh018 xx51 MET5 METMID.lef. Reading DECAP macros from LEF file. Reading DEF file frequency divider.def. . . Number of rows is 14 ongest row has width 83.475 um addspacers: No room for stripes, pitch reduced from 49770.0 to 34902.0. addspacers: Inserting 2 stripes of width 1.89 um (2.0 um requested) Pitch 34.902 um, offset 23.94 um stretch: Number of components is 264 Analysis of DEF file: Number of components = 236New number of components = 264 Number of rows = 14Stripe width 1890 fits 3 VIA1 X so at cut width 260.0 separation 260.0 Stripe width 1890 fits 3 VIA2 so at cut width 260.0 separation 260.0 Stripe width 1890 fits 3 VIA3 so at cut width 260.0 separation 260.0 Stripe width 1890 fits 3 VIA4 so at cut width 260.0 separation 260.0 stripe width 1890 fits 2 VIATP X so at cut width 360.0 separation 350.0 Adjusting obstructions for power striping Done with addspacers.tcl plifanno.tcl /home/elmioiti/design/P frequency divider/gflow/synthesis/frequency divider.blif frequency divi /home/elmioiti/design/P\_frequency\_divider/qflow/synthesis/frequency divider anno.bli Running blifanno.tcl

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### Qrouter:

/home/elmioiti/design/P frequency divider bak/qflow/log/route.log

Oflow route logfile created on Sat Aug 4 04:24:01 PDT 2018 grouter -nog -s frequency\_divider.cfg Qrouter detail maze router version 1.3.100.T Reading LEF data from file /ef/tech/XFAB.3/EFXH018C/libs.ref/techLEF/xh018 xx51 MET5 METMID.lef. LEF read: Processed 2312 lines. Multiple vertical route layers at different pitches. Using smaller pitch 0.63, will route on 1-of-N tracks if necessary. Reading LEF data from file /ef/tech/XFAB.3/EFXH018C/libs.ref/lef/D CELLS/xh018 D CELLS.lef. LEF file: Defines site core (ignored) LEF read: Processed 84298 lines. Multiple vertical route layers at different pitches. Using smaller pitch 0.63, will route on 1-of-N tracks if necessary. Reading DEF data from file frequency divider.def. Diagnostic: Design name: "frequency divider" Multiple vertical route layers at different pitches. Using pitch 0.63 and routing on 1-of-N tracks for larger pitches. Processed 264 subcell instances total. Processed 11 pins total. Processed 244 nets total. LEF Read, Line 1385: Via "VIA1 X so" does not define a metal layer! LEF Read, Line 1386: Via "VIA1 X so" does not define a metal layer! LEF Read, Line 1387: Via "VIA1 X so" does not define a metal layer! LEF Read, Line 1389: Via "VIA2 so" does not define a metal layer! LEF Read, Line 1390: Via "VIA2 so" does not define a metal layer! LEF Read, Line 1391: Via "VIA2 so" does not define a metal layer! LEF Read, Line 1393: Via "VIA3 so" does not define a metal layer! LEF Read, Line 1394: Via "VIA3 so" does not define a metal layer! LEF Read, Line 1395: Via "VIA3 so" does not define a metal layer! LEF Read, Line 1397: Via "VIA4 so" does not define a metal layer! LEF Read, Line 1398: Via "VIA4 so" does not define a metal layer! LEF Read, Line 1399: Via "VIA4 so" does not define a metal layer! LEF Read, Line 1401: Via "VIATP\_X\_so" does not define a metal layer! LEF Read, Line 1402: Via "VIATP X so" does not define a metal layer LEF Read, Line 1404: Via "VIA1 X so" does not define a metal layer! LEF Read, Line 1405: Via "VIA1 X so" does not define a metal layer! LEF Read, Line 1406: Via "VIA1\_X\_so" does not define a metal layer!

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12/24/2018 19

### POST STA

#### /home/elmioiti/design/P\_frequency\_divider\_bak/qflow/log/post\_sta.log

Oflow static timing analysis logfile created on Sat Aug 4 04:24:54 PDT 2018

Converting qrouter output to vesta delay format Running rc2dly -r frequency\_divider.rc -l /ef/tech/XFAB.3/EFXH018C/libs.ref/liberty/D\_CELLS/D\_CELLS\_LPMOS\_typ\_1\_80V\_25C.lib -d frequency\_divider.dly Converting qrouter output to SPEF delay format

Running rc2dly -r frequency\_divider.rc´-l /ef/tech/XFAB.3/EFXH018C/libs.ref/liberty/D\_CELLS/D\_CELLS\_LPMOS\_typ\_1\_80V\_25C.lib -d frequency\_divider.spef Converting grouter output to SDF delay format

Running rc2dly -r frequency\_divider.rc -l /ef/tech/XFAB.3/EFXH018C/libs.ref/liberty/D\_CELLS/D\_CELLS\_LPMOS\_typ\_1\_80V\_25C.lib -d frequency\_divider.sdf Running vesta static timing analysis with back-annotated extracted wire delays

vesta -c -d frequency\_divider.dly --long frequency\_divider.rtlnopwr.v /ef/tech/XFAB.3/EFXH018C/libs.ref/liberty/D\_CELLS/D\_CELLS\_LPMOS\_typ\_1\_80V\_25C.lib

Vesta static timing analysis tool (c) 2013-2017 Tim Edwards, Open Circuit Design

Parsing library "D\_CELLS\_LPMOS\_typ\_1\_80V\_25C" End of library at line 426120 Parsing module "frequency\_divider" Lib Read: Processed 426121 lines. Verilog netlist read: Processed 248 lines. Number of paths analyzed: 29

Top 20 maximum delay paths:

1693.9 ps

1865.4 ps

0

	9/CN to DFFQX4 12/D delay 2169 ps
1.1 p	
	s odd 0 initial begin 1 : DFFQX4 9/Q -> NO2X1 6/B
798.9 p	
987.9 p	
1322.2 p	
1578.2 p	
1988.4 p	
Path DFFQX4	11/CN to DFFQX4 13/D delay 1920.29 ps
2.2 p	in bF buf1: BUX2 8/Q -> DFFQX4 11/CN
617.3 p	s odd 0 initial begin 3 : DFF0X4 11/0 -> NO3X4 1/B
864.4 p	s149_: N03X4_1/Q -> AND3X4_1/A s155_: AND3X4_1/Q -> N02X2_3/A
1141.5 p	155 : AND3X4 1/Q -> N02X2 3/A
1309.9 p	s N02X2_3/Q -> A031X0_1/A
1833.8 p	s _36_5: A031X0_1/Q -> DFFQX4_13/D
ath DFFQX4	11/CN to DFFQX4 5/D delay 1836.62 ps
2.2 p	s in bF buf1: BUX2 8/Q -> DFFQX4 11/CN
617.3 p	s odd_0_initial_begin_3_: DFFQX4_11/Q -> NO3X4_1/B
864.4 p	s 149 : NO3X4 1/0 -> AND5X4 1/B
1353.2 p	s 83 : AND5X4 1/0 -> ON21X0 7/A
1574.6 p	87: 0N21X0 7/Q -> NA22X0 3/B
1898.3 p	s [87]: 0N21X0[7/Q -> NA22X0[3/B s [34_4]: NA22X0[3/Q -> DFFQX4_5/D
Path DFFQX4	_2/CN to DFFQX4_6/D delay 1819.72 ps
0.8 p	
	s odd_0_counter2_1_: DFFQX4_2/Q -> NO2X1_9/B
813.6 p	s
1078.3 p	
1402.0 p	91 : 0N21X0_8/Q -> A032X1_4/C
1890.5 p	s345_: A032X1_4/Q -> DFFQX4_6/D
Path DFFQX4	_11/CN to DFFQX4_4/D delay 1803.81 ps
2.2 p	
	s odd_0_initial_begin_3_: DFFQX4_11/Q -> NO3X4_1/B
864.5 p	s149_: N03X4_1/Q -> NA3X2_1/A
1090.8 p	5 71 : NA3X2 1/0 -> ON21X0 6/A
1368.3 p	s
1603 0 0	

80: NA22X0\_2/Q -> NA2X0\_16/A \_34\_3\_: NA2X0\_16/Q -> DFFQX4\_4/D

1392.8 ps	59 : NA2X0 13/Q -> MU2IX1 2/IN1
1617.7 ps	
1817.3 ps	_340_: MU2IX1_3/Q -> DFFQX4_1/D
Path DFFQX4	2/CN to DFFQX4_3/D delay 1429.15 ps
0.8 ps	in_bF_buf2: BUX2_7/Q -> DFFQX4_2/CN odd_0_counter2_1_: DFFQX4_2/Q -> ON21X0_5/B 66_: ON21X0_5/Q -> NO211X0_1/AN
621 4 ns	odd 0 counter2 1 : DEE0X4 2/0 -> ON21X0 5/B
889 5 ns	66 : 0N21X0 5/0 -> N02T1X0 1/AN
1188.9 ps	_67_: N02I1X0_1/Q -> NA2X0_14/B
1428.6 ps	60 : NA2YO 14/0 -> MU2TY1 6/TN1
1420.0 ps	$_{70}$ ; MU2TV1 6/0 > MU2TV1 7/TW1
1656.4 ps 1856.5 ps	
5. 	imum clock frequency (zero slack) = 461.041 MHz
	······
Number of pa	ths analyzed: 29
Top 20 minim	um delay paths:
Path DFRROX4	5/C to DFRRQX4_5/D delay 635.953 ps
0.9 ps	in bF buf0: BUX2 9/0 -> DFRROX4 5/C
481.7 ps	in_bF_buf0: BUX2_9/Q -> DFRRQX4_5/C even_0_counter_5_: DFRRQX4_5/Q -> AN31X1_1/D
545.1 ns	
545.1 ps 608.3 ps	_25_: N02X0_3/Q -> DFRRQX4_5/D
Path DFRSQX4	_1/C to DFRSQX4_1/D delay 670.547 ps
1.0 ps	in_bF_buf1: BUX2_8/Q -> DFRSQX4_1/C
	even 0 counter 0 : DERSOX4 $1/0 \rightarrow NA2T1X0 2/B$
490.4 ps	_13_: NA2I1X0_2/Q -> NA3X0_3/B
611.8 ps	_20_: NA3X0_3/Q -> DFRSQX4_1/D
Path DFRSOX4	2/C to DFRSQX4 2/D delay 710.343 ps
0.7 ps	
	even_0_out_counter: DFRSQX4_2/Q -> ON31X0_1/D
470.9 ps	
563.1 ps	_3_: NA2X0_2/Q -> DFRSQX4_2/D
Path DFROX4	4/C to DFRRQX4_6/D delay 722.591 ps
1.6 ps	in bF buf3: $BUX2 6/0 \rightarrow DFR0X4 4/C$
370 2 ns	odd 0 old N 3 · DEROX4 4/0 -> NO2X2 2/B
439.5 ps	odd_0_old_N_3_: DFRQX4_4/Q -> N02X2_2/B 136_: N02X2_2/Q -> N03I1X2_2/B
505.3 ps	_139_: NO3I1X2_2/Q -> AN32X1_1/B
625.9 ps	
	9/C to DFRQX4 9/D delay 733.052 ps
2.0 ps	
462 7 pc	add $\Theta$ counter 2 : DEPOVA $Q/Q > NO2V2 7/P$
402.7 ps	odd_0_counter_2_: DFRQX4_9/Q -> N02X2_7/B _107_: N02X2_7/Q -> N03X2_2/C
500.4 ps	_107_: NO2X2_7/Q -> NO3X2_2/C 109 : NO3X2 2/Q -> MU2IX1 8/IN1
636.2 ps 724.0 ps	
	11/CN to DFFQX4 11/D delay 753.119 ps
2 2 nc	in_bF_buf1: BUX2_8/Q -> DFFQX4_11/CN
400 1 pc	odd 0 initial begin 3 · DEFOX4 11/0 -> MO3Y2 1/P
400.1 ps 483.3 ps	in_bF_buf1: BUX2_8/Q -> DFFQX4_11/CN odd_0_initial_begin_3_: DFFQX4_11/Q -> NO3X2_1/B _40_: NO3X2_1/Q -> ON21X0_3/B
585.3 ps	
665.1 ps	
000.1 ps	_30_3 MAZAO_11/Q -> DFFQA4_11/D
	_4/C to DFRRQX4_4/D delay 761.078 ps
1.9 ps	in_bF_buf1: BUX2_8/Q -> DFRRQX4_4/C
436.8 ps	even_0_counter_4_: DFRRQX4_4/Q -> ON21X0_2/C _25_: ON21X0_2/Q -> NA3X0_7/C
543.4 ps	_25_: CN23X0_2/Q -> NA3X0_7/C
663.8 ps	_24_: NA5X0_7/Q -> DFRRQX4_4/D

Migration

С

DDX4 (1)       AND4X4 (1)         DDX1 (3)       ED2X1 (3)         D2X1 (3)       ED2X1 (3)         D2X1 (2)       NOZIX2 (2)         NZ (10)       BUX2 (10)         BX2 (2)       NA3X2 (2)         DXX (2)       NA3X2 (2)         DXX (2)       AN3X1 (2)         DXX (2)       AN3X1 (2)         DXX (2)       AN2XX1 (5)         DX2XX (2)       AN2XX0 (3)         DX2XX0 (3)       NA2XX0 (3)         DX1 (4)       AN3X1 (6)         DX2XX0 (1)       AN3X1 (6)         DX2XX0 (1)       AN3X1 (6)         DX2XX0 (1)       AN3X1 (4)         DX2XX0 (1)       AN3X1 (4)         DX2XX0 (1)       AN3X1 (4)         DX2XX0 (1)       AN3X1 (4)         DX2XX0 (1)       AN03X4 (1)         DX2X4 (1)       AN03X4 (1)         DXX4 (1)       AN03X4 (1)         DXX4 (2)       NA2XX1 (2)         DXX4 (1)       AN03X4 (1)         DXX4 (1)       AND3X4 (1)         DXX4 (1)       AND3X4 (1)         DXX4 (1)       AND3X4 (1)         DXX4 (1)       AND2XX4 (1)         DXX4 (1)       AND2XX4 (1)         DXX4 (1)	
1211X2 (2)       HO2IIX2 (2)         N22 (10)       BUX2 (10)         13X2 (2)       NA3X2 (2)         13X1 (2)       AN3X1 (2)         13X1 (2)       AN3X2 (2)         12XX1 (5)       AN2IX1 (5)         12XX1 (2)       AN2IX1 (2)         12XX0 (6)       NA2IX0 (6)         12XX1 (4)       AO2IX0 (1)         12XX1 (4)       AO3X1 (4)         1XX1 (4)       INX1 (4)         1XX1 (4)       AO3X1 (4)         1XX1 (4)       AO3X1 (4)         1XX1 (4)       AO3X1 (4)         1XX1 (4)       INX1 (4)         1XX1 (4)       AO3X1 (2)         1XX1 (4)       ANDSX4 (1)         1XX2 (2)       NOX4 (2)         1XX2 (1)       INX2 (1)         1XX4 (1)       AND3X2 (1)         1XX4 (1)       AN2X2 (1)         1XX4 (1)       AN312X1 (1)         1XX4 (1) <td< td=""><td></td></td<>	
D2IIX2 (2)       [N02IIX2 (2)         N22 (10)       [BUX2 (10)         B3X2 (2)       [NA3X2 (2)         B3X1 (2)       [AM3X1 (2)         B3X1 (2)       [AM3X1 (2)         B3X1 (5)       [AM2IX1 (2)         B3X1 (5)       [AM2IX1 (2)         B3X1 (6)       [AD22X0 (3)         B3X1 (6)       [AD21X0 (1)         D21X0 (1)       [AD21X0 (1)         D32X1 (4)       [AD32X1 (4)         D15X4 (1)       [AND5X4 (1]         D31X2 (2)       [AD31X2 (2)         D2X1 (1)       [AND2X4 (1]         D31X2 (2)       [AD2X1 (2)         D2X4 (2)       [AD2X4 (2)         D2X4 (2)       [AD2X4 (2)         D31X2 (1)       [AD2X4 (1)         D31X2 (1)       [AD32X1 (1)         D31X2 (1)       [AD32X1 (1)         D31X2 (1)       [AD32X1 (1)         D31X1 (1)       [AD32X1 (1)	
XX2 (10)     BUX2 (10)       XX1 (2)     NA3X1 (2)       XX1 (2)     AN3X1 (2)       XX2 (12)     AN2X1 (2)       XX2 (10)     NA2X1 (2)       XX2 (10)     NA2X1 (2)       XX2 (10)     NA2X1 (2)       XX1 (6)     NA3X1 (6)       XX2 (14)     AN2X1 (4)       XX2 (14)     AN3X1 (6)       XX2 (14)     AN3X1 (1)       XX2 (1)     AN3X4 (1)       XX2 (1)     INX1 (2)       XX2 (1)     INX2 (1)       XX1 (1)     INX2 (1)       XX1 (1)     IN	
GX2 (2)     NA3X2 (2)       ISIX (2)     AN3X2 (2)       IZIX (5)     AN2IX1 (2)       IZIX (5)     AN2IX1 (5)       IZIX (6)     NA2IX0 (6)       IZIX (6)     NA2IX0 (1)       IZIX (1)     IAO21X0 (1)       IZIX (1)     IAO21X0 (1)       IZIX (4)     INX1 (4)       IXIX (2)     NA3X2 (6)       IDSX4 (1)     INX1 (4)       IXX (2)     INX1 (4)       IXX (2)     INX1 (4)       IXX (2)     INX1 (4)       IXX (1)     ANDSX4 (1)       IDSX4 (1)     ANDSX4 (1)       IDSX4 (1)     INX2 (2)       IDSX4 (1)     INX2 (1)       IDX2 (1)     INX2 (1)       IDX2 (1)     INX2 (1)       IDX4 (1)     ANDX4 (1)       IDX2 (1)     INX2 (1)       IDX4 (1)     ANDX4 (1)       IDX2 (1)     INX2 (1)       IDX4 (1)     INX2 (1)       IDX4 (1)     INX2 (1)       IDX2 (1)     IAX22 (1)       IDX4 (1)     INX2 (1)       IDX2 (1)     IAX22 (1)	
ISIN (2)       AMSIN (2)         IZIN (5)       AMSIN (2)         IZIN (5)       AMZIN (5)         IZIN (6)       IMAZIN (6)         ISIN (6)       IMAZN (6)         ISIN (6)       IMAZN (6)         ISIN (6)       IMAZN (6)         ISIN (6)       IMAZN (6)         ISIN (4)       INX1 (4)         ISIN (2)       ISIN (2)         ISIN (2)       ISIN (2)         ISIN (2)       INAZ (1)         ISIN (2)       INAZ (1)         ISIN (2)       INAZ (1)         ISIN (1)       INAZ (1)	
121X1 (5)       AN21X1 (5)         122X1 (2)       AO22X1 (2)         121X0 (1)       INA21X0 (6)         121X0 (1)       INA21X0 (1)         132X1 (4)       INX1 (4)         RRQX4 (6)       IDFRQX4 (6)         ID5X4 (1)       INX1 (2)         IN31X2 (2)       IN031X2 (2)         RSQX4 (2)       IPFSQX4 (2)         IX2 (1)       INA21X1 (2)         IX2 (1)       INA21X1 (2)         IX2 (1)       INA21X1 (2)         IX2 (1)       INA21X2 (1)         IX2 (1)       INA21X1 (1)         IX2 (1)       INA21X2 (1)         IX2 (1)       INA21X1 (1)         IX2 (1)       INA1X2 (1)         IX2 (1)       INA1X2 (1)         IX2 (1)       INA21X1 (1)	
22211 (2)       A022X1 (2)         V211X0 (6)       NA211X0 (6)         V21X0 (1)       NA22X0 (3)         U3X1 (6)       NA3X1 (6)         U21X0 (1)       A021X0 (1)         V21X0 (1)       IOA21X0 (1)         V21X0 (1)       IOA21X0 (1)         V21X0 (1)       IOA21X0 (1)         V21X1 (4)       INX1 (4)         VX1 (1)       IAND5X4 (1)         VX1 (2)       INA21X1 (2)         VX2 (1)       INX2 (2)         RSQX4 (2)       INX2 (1)         VX2 (1)       INA2X2 (1)         VX2 (1)       INA2X2 (1)         VX2 (1)       INA32X1 (1)         V31X2 (1)       IOA31X2 (1)         V31X1 (1)       IOA31X0 (3)         V31X1 (1)       IOA31X0 (1)         V31X1 (1)       IOA21X1 (1)         V31X1 (2)       INA31X1 (2)         Imber of devices: 236       INumber of devices: 236	
V2IX0 (6)       NA2IX0 (6)         V2X0 (3)       NA22X0 (3)         V2X0 (1)       IA22X0 (1)         V2X0 (1)       IA021X0 (1)         V2X1 (4)       INX1 (4)         RRQX4 (6)       DFRRQX4 (6)         UD5X4 (1)       IAND3X4 (1)         V2X1 (2)       NO31X2 (2)         RSQX4 (2)       INO2X4 (2)         V2X4 (2)       INO2X4 (2)         V2X4 (2)       IAND2X4 (1)         V2X2 (1)       IAN2X2 (1)         V2X4 (1)       IAN2X2 (1)         V2X4 (1)       IAN2X4 (1)         V2X2 (1)       IAN2X2 (1)         V2X2 (1)       IAN2X2 (1)         V2X2 (1)       IAN2X2 (1)         V2X2 (1)       IAN2X2 (1)         V3IX0 (1)       IAN2X2 (1)         V3IX1 (2)       IAN2X2 (1)         V3IX1 (2)       IAN2X2 (1)         V3IX1 (1)       IAN2X2 (1)         V3IX1 (2)       IAN3IX0 (1)         V3IX1 (2)       IAN3IX0 (1)	
V22X0 (3)       INA22X0 (3)         U21X0 (1)       INA3X1 (6)         U21X0 (1)       INA3X1 (6)         U21X0 (1)       INA3X1 (6)         U21X0 (1)       INA3X1 (6)         U21X0 (1)       INA3X1 (4)         U21X0 (1)       INA3X1 (4)         U21X0 (1)       INA3X1 (4)         U21X0 (1)       INA3X1 (4)         U21X0 (1)       INX1 (4)         WA3X1 (4)       INX1 (4)         WA3X1 (1)       INX2 (1)         WA3X1 (1)       INX2 (2)         WX2 (1)       INX2 (1)         WX2 (1)       INX2 (1)         WA3X2 (1)       INX2 (1)         WA3X2 (1)       INX31X2 (1)         WA3X2 (1)       INX31X2 (1)         WA3X2 (1)       INX31X2 (1)         WA3X2 (1)       INX31X2 (1)         WA3X4 (1)       INX31X2 (1)         WA3X4 (1)       INX31X2 (1)         WA31X2 (1)       INX31X2 (1)         WA31X2 (1)       INX31X2 (1)         WA	
33X1 (6)       NA3X1 (6)         0211X0 (1)       A0211X0 (1)         021X0 (1)       0A21X0 (1)         032X1 (4)       A032X1 (4)         MADEL       AND5X4 (1)         MADEL       AND5X4 (1)         MADEL       AND5X4 (1)         MADEL       MADEL	
2211X0 (1)       A0221X0 (1)         221X0 (1)       OA21X0 (1)         221X0 (1)       OA21X0 (1)         32X1 (4)       A032X1 (4)         IX1 (4)       INX1 (4)         RRQM (5)       DFRRQX4 (6)         ID5X4 (1)       AND5X4 (1)         ID3X1 (2)       INX1 (2)         RRQV4 (2)       INX2 (2)         RSQX4 (2)       INX2 (1)         IX21X1 (2)       INX2 (1)         ID5X2 (1)       INX2 (1)         ID5X4 (1)       INX2 (1)         ID5X4 (1)       INX2 (1)         ID5X4 (1)       INA21X1 (2)         IX21X1 (2)       INX2 (1)         ID5X4 (1)       INA22X4 (1)         ID5X4 (1)       INA32X4 (1)         ID5X4 (1)       INA31X1 (1)         ID5X4 (1)       INA31X2 (1)         ID5X4 (1)       INA31X0 (1)         ID5X4 (1)       INA31X1 (2)         INS1X0 (1)       INA31X1 (2)         INS1X1 (2)       INA31X1 (2)         INS1X1 (1)       INA31X1 (2)	
V21X0 (1)       0A21X0 (1)         J32X1 (4)       INX1 (4)         J32X1 (4)       INX1 (4)         J32X1 (4)       INX1 (4)         J32X1 (4)       INX1 (4)         RRQX4 (6)       DFRRQX4 (6)         JDSX4 (1)       AND5X4 (1)         JD3X4 (1)       AND5X4 (1)         JD3X2 (2)       NO31X2 (2)         RRQX4 (2)       DFRSQX4 (2)         IX2 (1)       INX2 (1)         V2X4 (2)       NO2X4 (2)         J32X1 (1)       AND2X4 (1)         JD2X4 (1)       INA2Z2 (1)         JD2X4 (1)       INA2Z2 (1)         JD2X4 (1)       INA3I2X1 (1)         JD2X4 (1)       INA3I2X2 (1)         JD2X4 (1)       INA3I2X2 (1)         JD2X4 (1)       INA3I2X2 (1)         JD2X4 (1)       INA12X2 (1)         JD2X4 (1)       INA12X2 (1)         JD2X4 (1)       INA12X2 (1)         JD2X1 (1)       INA12X2 (1)	
332X1 (4)       INX1 (4)         IX1 (4)       INX1 (4)         IX1 (4)       INX1 (4)         IXX (4)       INX1 (4)         IXX (4)       IXX1 (4)         IXX (1)       IXX1 (4)         IDSX4 (1)       IXX1 (4)         IDSX4 (1)       IXX1 (4)         IDSX4 (1)       IXX1 (2)         IDSX4 (1)       IXX2 (2)         RSQX4 (2)       IXX2 (1)         IXX2 (1)       IXX2 (1)         IXX2 (1)       IXX2 (1)         IXX2 (1)       IXX2 (1)         IDSX4 (1)       AND2X4 (2)         ISZX1 (1)       IXX2 (1)         IDXX2 (1)       IXX2 (1)         IDXX4 (1)       IXX0 (3)         ISIX1 (1)       IXX0 (1)         ISIX2 (1)       IXX1 (1)         ISIX2 (1)       IXX0 (1)         ISIX2 (1)       IXX0 (1)         ISIX2 (1)       IXX0 (1)         ISIX2 (1)       IXX0 (1)         ISIX2 (1)       IXX1 (1)	
IX1 (4)       IXX1 (4)         FRRQX4 (6)       DFRRQX4 (6)         IDSX4 (1)       AND5X4 (1)         ID3X4 (1)       AND5X4 (1)         ID3X4 (1)       AND5X4 (1)         ID3X4 (2)       NO3X4 (2)         RSQX4 (2)       DFRSQX4 (2)         X2 (1)       INX2 (1)         VZ1X1 (2)       NAZIX1 (1)         ID4X2 (1)       AND2X4 (2)         ID4X2 (1)       AND2X4 (1)         ID4X2 (1)       NAZIX1 (1)         ID4X2 (1)       NAZIX1 (1)         ID4X2 (1)       NAZIX1 (1)         ID31X0 (3)       ONSIX0 (3)         IS1X0 (1)       ORSX4 (1)         IS1X0 (1)       ORSX4 (1)         IS1X0 (1)       ORSX4 (1)         IS1X2 (1)       NAZIX1 (1)         IS1X2 (1)       ORSX4 (1)         IS1X1 (2)       NAXIX0 (1)         IS1X2 (1)       OR2X1 (1)         IS1X1 (2)       NATIX1 (2)         Imber of nets: 246       Ne4>	
TRRQX4 (6)       IDFRRQX4 (6)         ID5X4 (1)       AND5X4 (1)         ID5X4 (1)       AND5X4 (1)         D311X2 (2)       N0311X2 (2)         RRQX4 (2)       INX2 (1)         IX2 (1)       INX2 (1)         V211X1 (2)       NA211X1 (2)         IX2 (1)       INX2 (1)         V21X4 (2)       NA21X1 (1)         ID2X4 (2)       INX2 (1)         ID2X4 (1)       AND3X4 (1)         ID2X4 (2)       INX2 (1)         ID2X4 (1)       AND2X1 (1)         ID2X4 (1)       AND312X4 (1)         ID2X4 (1)       INX22 (1)         SI2X1 (1)       INA312X1 (1)         ID2X4 (1)       INA312X1 (1)         ID2X4 (1)       INA31X0 (3)         SI2X1 (1)       INA31X0 (3)         SIX0 (1)       INA31X0 (1)         ISIX0 (1)       INA31X1 (2)         Imber of devices: 236       INumber of devices: 236         Imber of nets: 246       INumber of nets: 246         .rcuits match uniquely.       In         .rcuit : frequency_divider       Circuit 2: frequency_divider         .rcuit : frequency_divider       In         .rcuit : frequency_divider       In         .rcuit : frequency_di	
IDSX4 (1)       ANDSX4 (1)         IDSX4 (1)       ANDSX4 (1)         IDSX4 (1)       ANDSX4 (1)         IDSX4 (2)       NOTIX2 (2)         RSQX4 (2)       INX2 (1)         X2 (1)       ANDZX4 (2)         X4 (1)       ANDZX4 (1)         X2 (1)       ANDZX4 (1)         X2 (1)       ANDZX4 (1)         X2 (1)       ANDZX4 (1)         X2 (1)       INX2 (1)         X3 (1)       INX3 (3)         Y2 (1)       INX3 (3)         Y2 (1)       INX3 (1)         Y2 (1)       INX3 (2)         Y2 (1)       INX3 (1)         Y2 (1)       INX3 (2)         Y2 (1)       INX3 (2)<	
ID3X4 (1)       AND3X4 (1)         D3I1X2 (2)       NO3I1X2 (2)         RSQX4 (2)       DFRSQX4 (2)         IX2 (1)       INX2 (1)         V211X1 (2)       NAZIX1 (2)         U2X4 (2)       NAZIX1 (2)         I32X1 (1)       AND2X4 (2)         ID4X2 (1)       AND2X4 (2)         ID4X2 (1)       AND2X4 (1)         ID4X2 (1)       AND2X4 (1)         ID4X2 (1)       AND2X4 (1)         ID4X2 (1)       NAJIXX1 (1)         ISIX0 (3)       ORSX4 (1)         ISIX0 (1)       INAJIXX1 (2)         IN22 (1)       NAJIXX1 (2)         IN21 (1)       ORZX1 (1)         ISIX1 (2)       NAJIX1 (2)         Imber of devices: 236       Number of nets: 246         .rcuits match uniquely.	
REQX4 (2)     IDFRSQX4 (2)       IX2 (1)     INX2 (1)       IX2 (1)     INX2 (1)       IX2 (2)     NA2IX1 (2)       IX2 (1)     INX2 (1)       ID4X2 (1)     INX2X (1)       ID4X2 (1)     INX2X (1)       ID4X2 (1)     INX2X (1)       ID2X4 (1)     INX2X4 (1)       ID2X4 (1)     INX2X4 (1)       ID2X4 (1)     INX2X2 (1)       ID2X4 (1)     INX2X2 (1)       ISIX0 (3)     ION3IX0 (3)       ISIX0 (1)     INX3IX1 (2)       ISIX2 (1)     INX3IX1 (2)       IMAEX2 (1)     INX3IX1 (2)       IMAEX2 (1)     INX3IX1 (2)       Imber of devices: 236     INumber of devices: 236       Imber of nets: 246     INumber of nets: 246       .rcuits match uniquely.     INX4>       etlists match uniquely.     In       .dticcuit pins:     In       .rcuit 1: frequency_divider     Circuit 2: frequency_divider       .dt     In       .dt     In <tr< td=""><td></td></tr<>	
X2 (1)       INX2 (1)         V21X1 (2)       NA2I1X1 (2)         V2X4 (2)       NA2X4 (2)         J32X1 (1)       AN32X1 (1)         ID4X2 (1)       AN32X1 (1)         ID4X2 (1)       AND4X2 (1)         J32X4 (1)       AND2X4 (1)         J31ZX4 (1)       NA3I2X1 (1)         J31ZX4 (1)       NA3I2X1 (1)         J31ZX4 (1)       NA3I2X1 (1)         J31ZX1 (1)       NA3I2X1 (1)         J31X0 (3)       ON31X0 (3)         SX4 (1)       OR5X4 (1)         J31X0 (1)       A031X0 (1)         J31X1 (2)       NA3IZX1 (1)         J31X1 (2)       NA3IX1 (2)         Imber of devices: 236       Number of devices: 236         Imber of nets: 246       Number of nets: 246         .rcuits match uniquely.       N41         .rcuits match uniquely.       Int         .rcuit 1: frequency_divider       [Circuit 2: frequency_divider         .rcuit 2: frequency_divider       Int         .rcuit 2: frequency_divider       [and 1]         .rcuit 1: frequency_divider       [and 1]         .rcuit 2: frequency_divider       [and 1]         .rcuit 2: frequency_divider       [and 1]         .rcuit 3: frequency_divider <td></td>	
V2I1X1 (2)       NA2IIX1 (2)         V2X4 (2)       NO2X4 (2)         V2X4 (2)       AN32X1 (1)         V2X4 (2)       AN32X1 (1)         V2X4 (1)       AN32X1 (1)         V2X4 (1)       AN32X4 (1)         V2X4 (1)       AN32X4 (1)         V2X4 (1)       NA312X4 (1)         V2X2 (1)       NA312X1 (1)         V31X1 (1)       NA312X1 (1)         V31X2 (1)       NA312X1 (1)         V31X0 (3)       OM31X0 (3)         V31X0 (1)       A031X0 (1)         V31X1 (1)       OAS1X0 (1)         V31X1 (1)       OAS1X0 (1)         V21X1 (1)       OAS1X0 (1)         V31X1 (2)       NA31X1 (2)         mber of devices: 236       Number of nets: 246         rcuits match uniquely.       Number of nets: 246         rcuits match uniquely.       N<4>         vt       out         v0>       N<4>         vt       N<4>         vt       N<4>         vt       N<4>         vd       N<4>         vd       In         vd       In         vd       In         vd       In         vd	
22X4 (2)       MO2X4 (2)         332X1 (1)       AND2X4 (1)         104X2 (1)       AND2X4 (1)         102X4 (1)       AND2X4 (1)         102X4 (1)       NAD2X4 (1)         102X4 (1)       NAD2X4 (1)         102X4 (1)       NAD2X4 (1)         102X4 (1)       NAD2X4 (1)         102X1 (1)       NA3IZX1 (1)         31X0 (3)       ONSIX0 (3)         15X4 (1)       ORSX4 (1)         31X0 (1)       AO3IX0 (1)         13I2X2 (1)       NA3IZX2 (1)         13I2X1 (1)       ORSX4 (1)         31X0 (1)       AO3IX0 (1)         13I2X1 (1)       ORSX4 (1)         13I2X2 (1)       NA3IXX1 (2)         12X1 (1)       OR2X1 (1)         13IX1 (2)       NA3IXI1 (2)         Imber of devices: 236       Number of nets: 246         .rcuit smatch uniquely.	
332X1 (1)       AN32X1 (1)         ID4X2 (1)       AND4X2 (1)         ID2X4 (1)       AND2X4 (1)         3312X4 (1)       NO312X4 (1)         3312X4 (1)       NA312X1 (1)         3312X4 (1)       NA312X1 (1)         3312X1 (1)       OR5X4 (1)         3312X1 (1)       OR5X4 (1)         3312X1 (1)       OR5X4 (1)         3312X1 (1)       OR5X1 (1)         3312X1 (1)       OR5X1 (1)         3312X1 (1)       OR21X1 (1)         3312X1 (1)       OR21X1 (1)         311X1 (2)       NA31IX1 (2)         mber of nets: 246       Number of nets: 246        ccuits match uniquely.         ccuit pins:         ccuit pins:         ccuit pins:         ccuit 1: frequency_divider <td< td=""><td></td></td<>	
ID4X2 (1)       AND4X2 (1)         ID2X4 (1)       AND2X4 (1)         ID2X4 (1)       IN0312X4 (1)         ID2X2 (1)       IN42X2 (1)         ID2X2 (1)       INA312X1 (1)         ID2X4 (1)       INA312X1 (1)         ID2X4 (1)       INA312X1 (1)         ID2X2 (1)       INA312X1 (1)         ID2X0 (1)       ID4X0 (3)         ID4X0 (1)       ID4X0 (1)         ID4X2 (1)       ID4X0 (1)         ID4X0 (1)       ID4X0 (1)         ID4X1 (1)       ID4X1X1 (1)         ID4X1 (1)       ID4X1X1 (1)         ID4X1 (1)       ID4X1X1 (2)         Imber of devices: 236       Number of devices: 236         Imber of nets: 246       Number of nets: 246         Incuits match uniquely.       In         wbcircuit pins:       Incuit 2: frequency_divider         .rcuit 1: frequency_divider       Circuit 2: frequency_divider         .dt       In	
ID2X4 (1)       IAND2X4 (1)         D312X4 (1)       NO312X4 (1)         D312X4 (1)       NA312X1 (1)         D312X1 (1)       IAN312X1 (1)         B1X0 (3)       OR5X4 (1)         D312X2 (1)       IAN312X1 (1)         B1X0 (3)       OR5X4 (1)         D312X2 (1)       IAN312X1 (1)         D312X2 (1)       IAN312X2 (1)         D312X2 (1)       IAN312X2 (1)         D312X1 (1)       OR2X1 (1)         D31X1 (2)       IAN31X1 (2)         Imber of devices: 236       Number of nets: 246         .rcuits match uniquely.       INumber of nets: 246         .rcuits match uniquely.       In         .rcuit 1: frequency_divider       Circuit 2: frequency_divider         .rcuit 1: frequency_divider       Icurcuit 2: frequency_divider         .rcuit 1: frequency_divider       In         .rcuit 1: frequency_divider       In         .rcuit 1: frequency_divider       In         .rcuit 2: frequency_divider       In         .rcuit 3: frequency_divider       In         .rcuit 1: frequency_divider       In         .rcuit 1: frequency_divider       In         .rcuit 1: frequency_divider       In         .rcuit 2: frequency_divider	
3312X4 (1)       NO312X4 (1)         V2X2 (1)       NA2X2 (1)         V312X1 (1)       NA312X1 (1)         V31X0 (3)       ON31X0 (3)         V31X1 (1)       OR5X4 (1)         V31X0 (1)       A031X0 (1)         V31X1 (1)       OR5X4 (1)         V31X2 (1)       A031X0 (1)         V31X2 (1)       OR5X4 (1)         V2X1 (1)       OR21X1 (1)         V2X1 (1)       OA21X1 (1)         V2X1 (1)       OA21X1 (1)         V31X1 (2)       NA311X1 (2)         mber of devices: 236       Number of nets: 246        cruits match uniquely.       Number of nets: 246        cruits match uniquely.         detrouge         detrouge <t< td=""><td></td></t<>	
V2X2 (1)       NA2X2 (1)         V2X2 (1)       NA2X2 (1)         V2X2 (1)       NA3I2X1 (1)         V2X2 (1)       OM3IX0 (3)         V2X4 (1)       OM3IX0 (3)         V2X4 (1)       OM3IX0 (1)         V2X2 (1)       NA3I2X2 (1)         V2X1 (1)       OA2X1 (1)         V2X1 (1)       OA2         vdi       requery         vdit       requery      <	
3IZX1 (1)       NA3IZX1 (1)         IX0 (3)       ON31X0 (3)         SX4 (1)       OR5X4 (1)         J31X0 (1)       A031X0 (1)         BI2X2 (1)       NA3IZX2 (1)         VZX1 (1)       OR2X1 (1)         VZX1 (1)       OR2X1 (1)         VZX1 (1)       OR2X1 (1)         VZX1 (1)       OR2X1 (1)         VILX1 (1)       OR2X1 (1)         VILX1 (1)       OR2X1 (2)         Imber of devices: 236       Number of devices: 236         Imber of nets: 246       Number of nets: 246         .rcuits match uniquely.	
I3IX0 (3)       [ON3IX0 (3)         ISX4 (1)       IORSX4 (1)         ISX0 (1)       IA03IX0 (1)         ISIX0 (1)       IA03IX1 (1)         ISIX1 (1)       IA03IX1 (2)         Imber of devices: 236       Number of nets: 246         Incuits match uniquely.       Int         It       Int         It       Int         In       Int         Int       Int         In	
SX4 (1)       ORSX4 (1)         D31X0 (1)       A031X0 (1)         D31X0 (1)       NA31X2 (1)         D31X2 (1)       NA31X2 (1)         U2X1 (1)       OR2X1 (1)         V2X1 (1)       OA21X1 (1)         U3IX1 (2)       NA31IX1 (2)         Imber of devices: 236       Number of devices: 236         Imber of nets: 246       Number of nets: 246         rcuits match uniquely.	
331X0 (1)       A031X0 (1)         331X2 (1)       NA312X2 (1)         331X1 (1)       OR2X1 (1)         321X1 (1)       OR2X1 (1)         321X1 (2)       NA311X1 (2)         mber of devices: 236       Number of devices: 236         mber of nets: 246       Number of nets: 246         .rcuits match uniquely.          ttlists match uniquely.          .rcuit pins:          .rcuit 1: frequency_divider       Circuit 2: frequency_divider <td< td=""><td></td></td<>	
N3I2X2 (1)     NA3I2X2 (1)       N2X1 (1)     OA2X1 (1)       N2IX1 (1)     OA2XX1 (1)       Number of devices: 236     Number of nets: 246       Imber of nets: 246     Number of nets: 246       Incuits match uniquely.     Number of nets: 246       Incuits match uniquely.     Incuit 2: frequency_divider       Incuit 1: frequency_divider     Circuit 2: frequency_divider       Incuit 1: frequency_divider     N<4>       N<	
1221 (1)       OR221 (1)         121X1 (1)       OA21X1 (1)         13IX1 (2)       NAJIX1 (2)         Imber of devices: 236       Number of devices: 236         Imber of nets: 246       Number of nets: 246         rcuits match uniquely.       Intervention         atlists match uniquely.       Intervention         ibcircuit pins:       Circuit 2: frequency_di         rcuit 1: frequency_divider       [Circuit 2: frequency_di         it       Jout         roos       N<4>         out       N<0>         eset       reset         in       Int         3>       N<3>         id       gnd! **Mismatch**         id       vdd! **Mismatch**         id       vdd! **Mismatch**         id       vdd! **Mismatch**         id       in         id       vdd! **Mismatch**         id       vdd! **Mismatch**         id       vd2>	
k21X1 (1)       OA21X1 (1)         k3I1X1 (2)       NA3I1X1 (2)         mber of devices: 236       Number of devices: 236         mber of nets: 246       Number of nets: 246         .rcuits match uniquely.	
33IX1 (2)       NA3IX1 (2)         imber of devices: 236       Number of nets: 246         imber of nets: 246       Number of nets: 246         .rcuits match uniquely.	
imber of devices: 236       Number of devices: 236         imber of nets: 246       Number of nets: 246         intervalue       Number of nets: 246         int       Circuit 2: frequency_divider         int       Int         int <td< td=""><td></td></td<>	
Imber of nets: 246     Number of nets: 246       rcuits match uniquely.     Init of the second seco	
.rcuits match uniquely.         ttlists match uniquely.         .bcircuit pins:         .rcuit 1: frequency_divider	
bcircuit pins: rcuit 1: frequency_divider Circuit 2: frequency_divider 4> N<4> out 0> N<4> 10 10 10 10 10 10 10 10 10 10	
rcuit 1: frequency_divider     [Circuit 2: frequency_divider]       4>     N<4>       4>     out       4>     out       4>     N<4>       10     In       4>     N<4>       11     N<1>       12     N<1>       13     In       14     Ignd! **Mismatch**       15     N<5>       16     Vdd! **Mismatch**       17     N<2>	
it     out       40>     N<40>       sset     reset       <1>     N<1>       n     in       3>     N<3>       nd     Ignd! **Mismatch**       id     Vdd! **Mismatch**       5>     N<5>       <2>     N<2>	ivider
x0>     N<0>       sset     reset       x1>     N<1>       n     in       x3>     N<3>       nd     gnd! **Mismatch**       id     ydd! **Mismatch**       x5>     N<4>       x2>     N<2>	
eset     reset       (1>)     N<1>       1     1       (3>)     N<3>       Nd     [gnd! **Mismatch**       Nd     Vdd! **Mismatch**       S>     N<5>       <2>     N<2>	
<pre>&lt;1&gt;  N&lt;1&gt; in 3&gt;  N&lt;3&gt; dd  gnd! **Mismatch** dd  ydd! **Mismatch** 5&gt;  N&lt;5&gt; &lt;2&gt;  N&lt;5&gt; &lt;2&gt;  N&lt;2&gt;</pre>	
in 3>  N<3> id  gnd! **Mismatch** id  ydd! **Mismatch** 5>  N<5> -2>  N<2> ell pin lists are equivalent. T	
3>     N<3>       1d     [gnd! **Mismatch**       1d     Vdd! **Mismatch**       5>     N<5>       2>     N<2>	
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ell pin lists are equivalent. 📅	
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DRC : 4 errors . Minor fixes required!

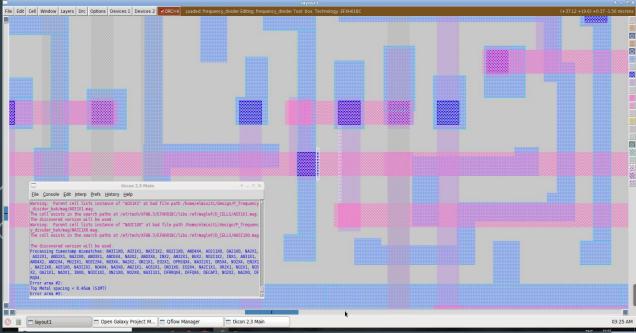
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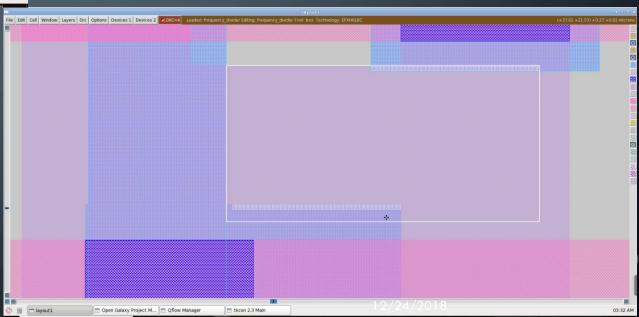
🗖 Open Galaxy Project M... 🔲 Qflow Manager

Options Devices 1 Devices 2 DRC=4

v Manager 📃 🗖 tkcon 2.3 Main

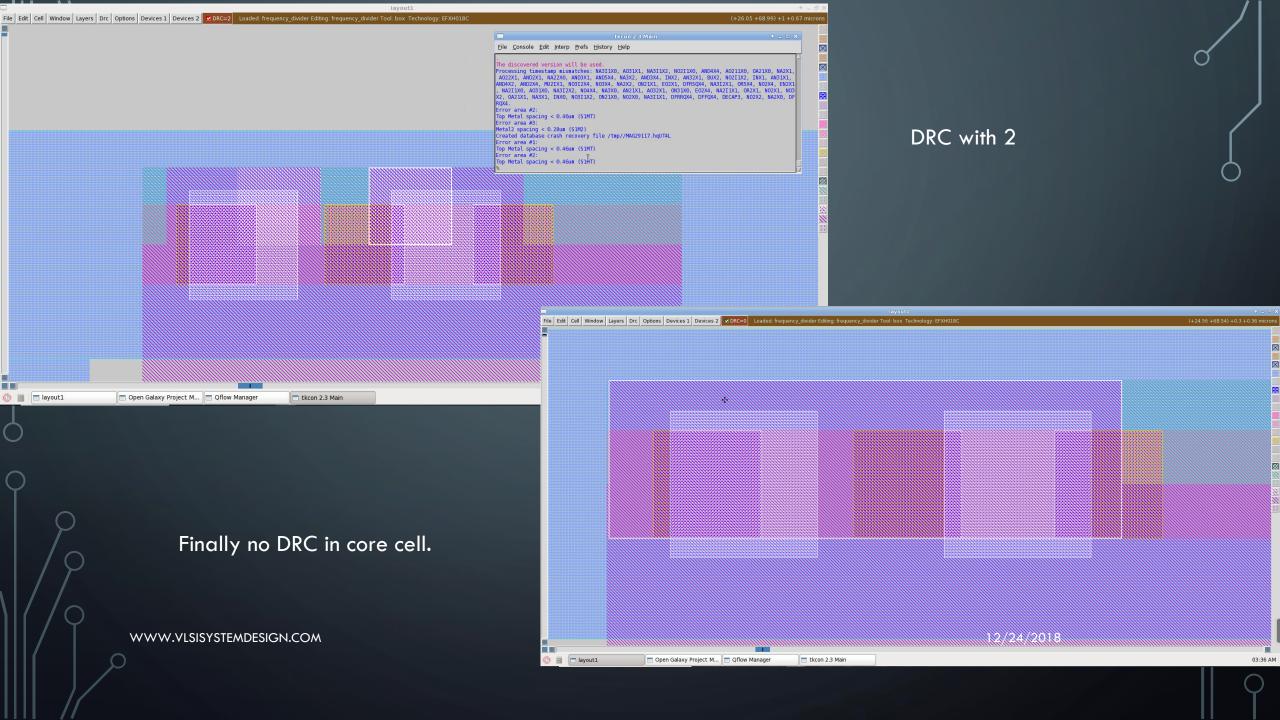
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DRC=0 Loaded: frequency\_divider Editing: frequency\_divider Tool: box Technology: EFXH018(

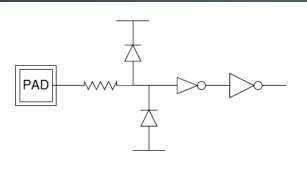
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# I/O PADS & INTERCONNECTIONS



 ✓ DRC=8
 Loaded: frequency\_divid Editing: frequency\_divid Tool: box Technology: EFXH018C

CORNERESDF	VDDPADF	VDDOHPADP	CORNERESDF
CORNERESDF_1	VDDPADF_0	VODORPADE_0	CORNERESDF_0
ICF ICF_0			ICF ICF_7
ICF ICF_1			BT4F BT4F_0
ICF ICF_2			ICF ICF_5
ICF ICF_3			ICF ICF_4
CORNERESDF	ICF	GNDORPADF	CORNERESDF
CORNERESDF_2	ICF_6	GNDORPADE	

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\* \_ 0 ×

tkcon 2.3 Main

Eile Console Edit Interp Prefs History Help

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# POWER & GROUND CONNECTIONS

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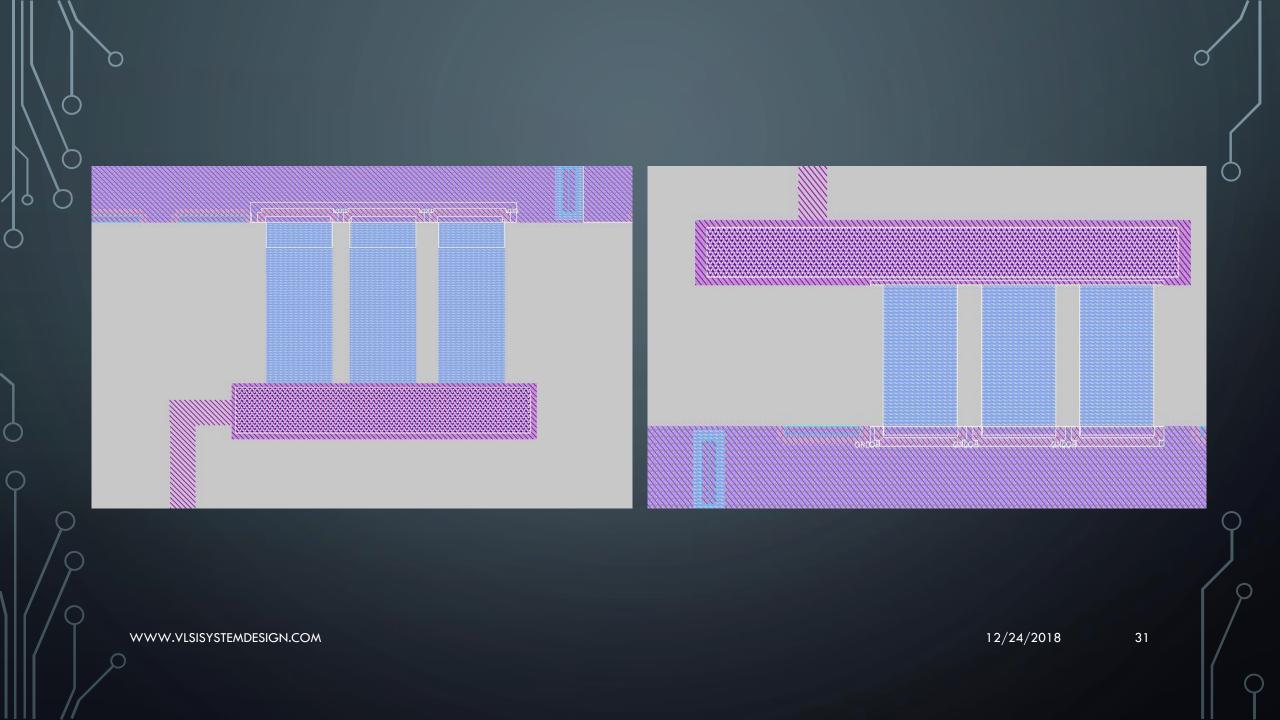
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	tkcon 2.3 Mais Ele <u>Console Edit Interp Prefs History Help</u> Sastehing to PCK Koni. Sastehing to PCK Koni. Sapant <b>sl.a2,a3,e4,a5,atp</b>	+ - ¤×		tkcon 2.3 Main       Ele Console Edit interp Prefs History Help       Switching to ROX tool.       t paint til.2, #3, #4, #5, #tp       paint via, via2, via3, via4, viatp	* - • ×
	tkcon 2.3 Main EVe Console Edd Interp Brefs History Help Switching to BOX tool. V paint sl.s2,s3,s44,s5,stp S	+ _ 0 X		tkcon 2.3 Main Ele Console Edit Interp Brefs History Help	* - ¤ ×
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Switching to BOX tool. % paint m1,m2,m3,m4,m5,mtp %		A M	Switching to BOX tool. % paint m1,m2,m3,m4,m5,mtp % paint via,via2,via3,via4,viatp		

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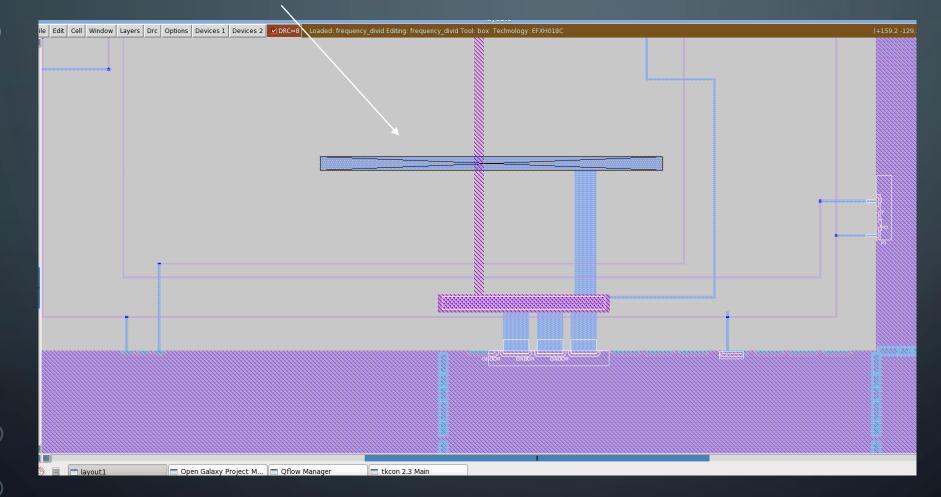
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# SUBSTRATE CONNECTIONS TO GND PAD

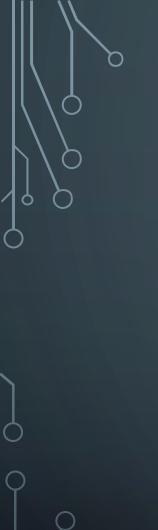


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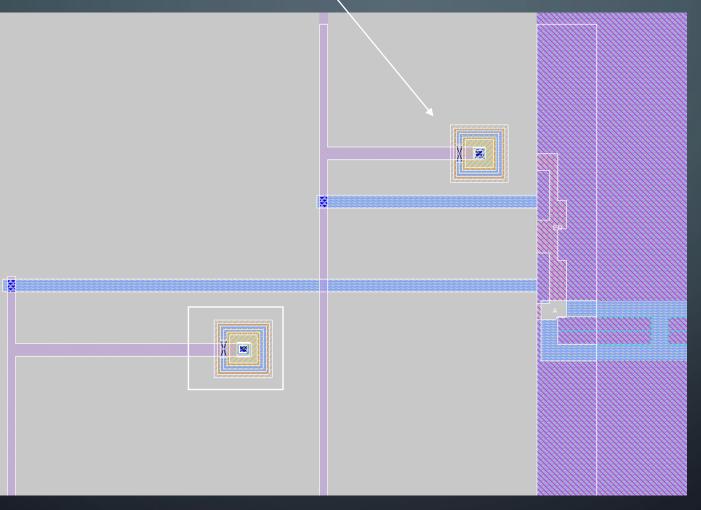
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# PI CONNECTIONS TO GROUND FOR LVS

			libmgr	↑ _ □ X
Load	Place	Pick		🔽 Filter
			Cell	Technology
▶./				
 v /ci/ccc			BC/libs.ref/maglef/primdev/	
→ /ef/tec	h/XFAB.3	/EFXH01	BC/libs.ref/maglef/D_CELLS/	
LGC	FX8			EFXH018C
LOC	GIC0			EFXH018C
LOC	GIC1			EFXH018C
LSG	CNX0			EFXH018C
LSG	GCNX1			EFXH018C
 LSG	CNX2			EFXH018C
LSG	GCNX3			EFXH018C
LSG	GCNX4			EFXH018C
Target wi	ndow: d	efault		



# ANTENNA DIODE



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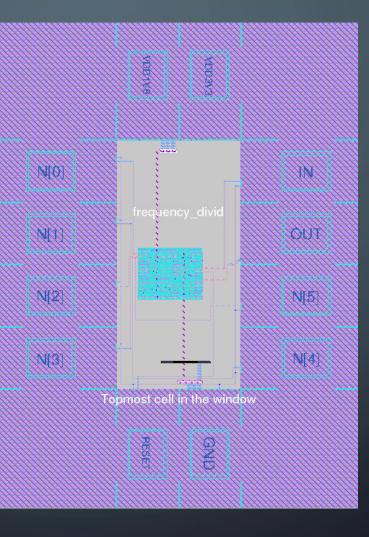
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# LVS : LAYOUT VS VERILOG NETLIST IN RUN LVS TOOL

Line	Layout:			S	hematic:	Terminal - elmioiti@centos:~/desig	n/frequency_divid/verlig	↑ - □ ×
⊽ 1	frequency_divid			fr	equency_divid	<u>T</u> erminal <u>G</u> o <u>H</u> elp		
⇒ 2	frequency_divid Summary				quency_divid Summary			
3	frequency_divid Devices				quency_divid Devices			
4	CORNERESDF(4)				DRNERESDF(4)	equency_divider.vgl"		
5	GNDORPADF(1)				IDORPADF(1)	<pre>/tech/XFAB.3/EFXH018C/libs.re</pre>		SV V
6	ICF(8) BT4F(1)				F(8) 4F(1)	<pre>//tech/XFAB.3/EFXH018C/libs.re</pre>	f/verilog/I0_CELLS_F3V/VLG_PRIMIT1	IVES V
0	VDDORPADF(1)				DORPADF(1)	equency_divider.v"		
9	VDDPADF(1)				DPADF(1)	≥n . v "		
10	dn(2)			dr		J . V "		
11	LOGIC0(1)				GIC0(1)	"ines.v"		
12	frequency_divider(1)			fre	quency_divider(1)			
13	frequency_divid Nets			fre	quency_divid Nets	Jency_divid (		
14	32			32		2		
Run						10, 10,000		
						(DDIV8,		
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Class: BT4F	instances:	1				tivider		
Class: CORNERE Class: LOGICO	SDF instances:	4				N <sub>.x</sub>		
Class: LUGICO Class: GNDORPA		1						
Class: VDDPADF	instances:	1						
Class: ICF Class: dn	instances: instances:	8						
Class: VDDORPA	DF instances:	ĩ						
ircuit contains	32 nets, and 5 disconnect	ed pins.				11/0		
	ns 20 elements, Circuit 2					J1V8;		
ircuit 1 contain	ns 32 nodes, Circuit 2	contains 32 nodes.				1343;		
Circuits match w	vith 1 symmetry.							
Vetlists match w	ith 1 symmetry.					23.		
ircuits match c	orrectly.	1_14901	noncennoideoigni _raven	ALAD . LI ANUTOC	IIII Wiro	THE		
		P raven spi	/home/elmioiti/design/P raven spi	XFAB : EFXH018C	wire			
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		freq divid1	/home/elmioiti/design/freq_divid1	XFAB : EFXH018C				
		frequency_divid	/home/elmioiti/design/frequency_div	XFAB : EFXH018C				
		my backup 15092018	/home/elmioiti/design/my_backup_15	(default)		SERT	30,1	Тор

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VSDOpen Conference 2018

## RAPID PHYSICAL IC IMPLEMENTATION AND INTEGRATION USING EFABLESS PLATFORM

ALBERTO GOMEZ SAIZ (AGS@DISROOT.ORG)

MSC. IMPERIAL COLLEGE LONDON

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VSDOpen Conference 2018

#### ABSTRACT

- Bio
- Project description
- Backend flow
  - Physical implementation
  - Top level integration
- Q&A

### BIO

- MSc. IC Design, Imperial College London
- Analog IC Designer (>5y)
  - IoT & connectivity
  - Low power data converters
  - Mixed signal design: PLL, ADC
  - Top level chip integration
  - Coder and open-source community member







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### PROJECT DESCRIPTION

- Digital Backend flow for a small RTL design
- Efabless platform
  - Free to access
  - Cloud based
  - Uses open-source tools
- IP:
  - Frequency Divider RTL from Efabless catalog
  - 0.18um XFAB 6M



- Digital frequency divider from Open Cores, by Joe Crop. Features:
- Selectable division word size in verilog definition
- IP Type: Hard IP
- Category: Divider
- Vendor: efabless · Contact
   Node: 180nm · Stage: Layout
- Foundry: X-FAB Certifications:
- Process: EFXH018C
   More Info
- Designer: efabless engineering License:
  - Contact Designer
    - 2/24/2018



#### BACKEND FLOW OVERVIEW

#### • From RTL to Tapeout:

- Synthesis (CloudV)
- Placement (qflow GUI)
- STA & Routing (qflow GUI)
- LVS & DRC (qflow GUI)
- Top level integration (Magic VLSI)
- Top level verification (LVS Manager)

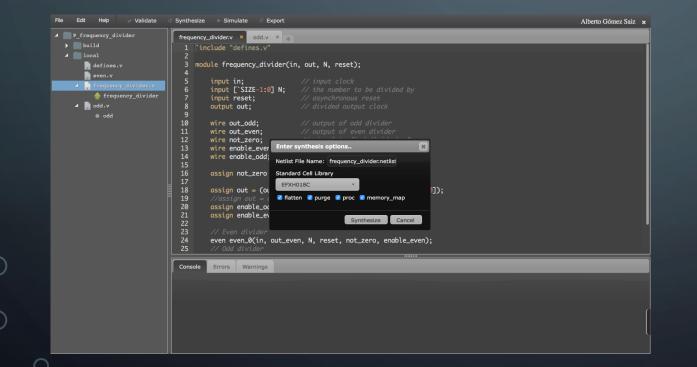
User: agomezs2				
Project: frequency_divi	der /home/nw	aignis/design/P	_frequency_divid	ler
Checklic Select new proje	ct			Synthesis Preparation
Preparation	(not done)	Run	Settings	Technology: EFXH018C
Synthesis	(not done)	Run	Settings	Standard cell set: EFXH018C Verilog module: frequency_divider
Placement	(not done)	Run	Settings	
Static Timing Analysis	(not done)	Run	Settings	
Routing	(not done)	Run	Settings	
Post-Route STA	(not done)	Run	Settings	
Migration	(not done)	Run	Settings	
LVS	(not done)	Run	Settings	
DRC	(not done)	Run	Settings	
Cleanup	(not done)	Run	Settings	

Status: no project\_vars.sh file, or no source directory, or no verilog file. Status set to "prep" Current qflow project status is: prep

Close Help

#### PHYSICAL IMPLEMENTATION: SYNTHESIS

#### • CloudV: Digital simulator + Synthesis tool



1		
2	11. Printing statistics.	
3	<i>c</i> 11.1.1	
4	<pre>=== frequency_divider ===</pre>	
5	Number of using a	104
6 7	Number of wires:	184
8	Number of wire bits:	234 184
9	Number of public wires: Number of public wire bits:	234
9 10	Number of public wire bits: Number of memories:	
11		0 0
12	Number of memory bits: Number of processes:	0
13	Number of cells:	226
14	AN21X0	5
15	AN31X0	2
16	AN32X0	1
17	AND2X0	3
18	AND3XØ	4
19	AND4X0	2
20	AND5X0	1
21	A0211X0	1
22	A022X0	2
23	A031X0	2
24	A032XØ	4
25	DFFQXØ	13
26	DFRQXØ	13
27	DFRRQXØ	6
28	DFRSQXØ	2
29	EN2X0	5
30	E02XØ	5
31	INXØ	21
32	MUZIXØ	8

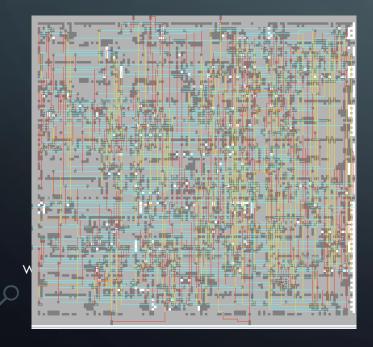
### PHYSICAL IMPLEMENTATION: PLACEMENT

- Define block aspect ratio
- Specify Power Stripes
  - Requires power estimation
- Create placement and arrangement pin constrains (GUI)

	🔲 Open Galaxy Oflow Pin Manager 🔶 🗆 🗙
Placement Settings	N_vector Top: Right: Bottom: 🛪 Left: 🛪 Permute: Start %: 0 Stop
Initial density: 1.0	N<0> × Fixed
Aspect ratio: 1.0	N <u> × FIXED</u>
Create power stripes: 🛪	N<1> × Fixed
Stripe width: 2.0	N<2> ▼ Fixed
Stripe pitch: 50.0	No. 2
Add extra space for power stripes: 🛪	N<3> ≭ Fixed
Arrange Pins	N<4> × Fixed
Placement graphic view: 🛪	N<5> x Fixed
	<i>inputs</i> Top: □ Right: □ Bottom: □ Left: ▼ Permute: ▼ Start %: 0 Stop %:
	Close Apply New Group Delete Group - Auto Group

#### PHYSICAL IMPLEMENTATION: STA & ROUTING

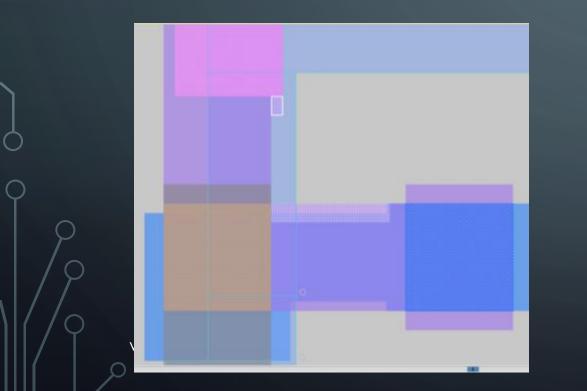
- STA -> max. freq of the design and worst delay path
- Specify number of metal layers for routing
- Post-Route STA recalculates max freq. with routing parasitics

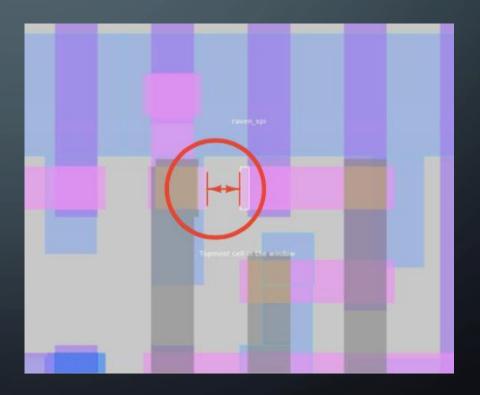


0.0 ps	even 0 counter 2			DFRRQX4_2/C
A DOMESTIC STRUCTURE S		_		
765.9 ps	_	_		ON31X0_1/B
1124.2 ps				NA2X0_2/A
1362.1 ps	_3	3_: NA2X	0_2/Q ->	DFRSQX4_2/D
omputed maxi	mum clock frequer	ncy (zero	slack) =	471.809 MHz

### PHYSICAL IMPLEMENTATION: DRC & LVS

• Using Magic VLSI fix LVS and DRC errors (if any)





#### PHYSICAL IMPLEMENTATION: COMPLETED

rrequency divider.

Jser: agomezs2				
Project: frequency_divid	er /home/a	ddenoew/design/	P_frequency_divider	
Checklist				Cleanup Settings
Preparation	Okay	Run	Settings	Purge:
Synthesis	Okay	Run	Settings	
Placement	Okay	Run	Settings	
Static Timing Analysis	Okay	Run	Settings	
Routing	Okay	Run	Settings	
Post-Route STA	Okay	Run	Settings	
Migration	Okay	Run	Settings	
LVS	Okay	Run	Settings	
DRC	Okay	Run	Settings	
Cleanup	Okay	Run	Settings	
Current qflow project stat Current qflow project stat Current qflow project stat	us is: clean			

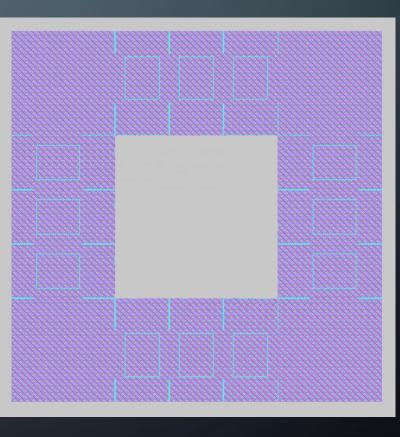
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#### TOP LVL INTEGRATION: PAD RING

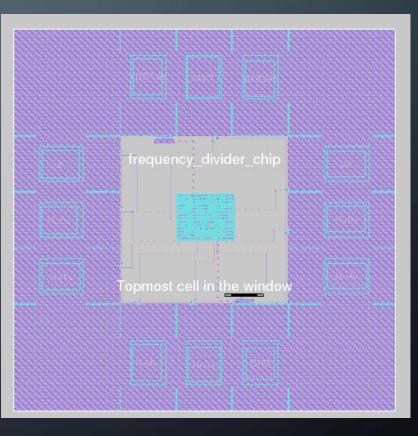
#### • Generate the pad ring

- Select pads based on IN/OUT requirements
- Use foundry cells (ESD protected)
- If design core limited uses fillers



### TOP LVL INTEGRATION: ROUTING

- Connect pins to pads
- Connect power busses to pads
- Add global substrate contact
- Add antenna diodes to digital outputs



### TOP LVL INTEGRATION: LVS

#### • Verify Top-level connectivity

User: agomezs2 Project: frequency_divider_chip /home/nwaignis/design/frequency_divider_chip Layout: frequency_divider_chip Verilog netlist: frequency_divider_chip subckt frequency_divider vdd gnd in N<0> N<1> N<2> N<3> N<4> N<5> reset out w_n + vdd DPT5741817_n1073741817# + vdd MDF50X4_5 BUX2_7/0 vdd gnd NA22X0_3/0 INX0_9/A DFF0X4 KENX1_2 gnd vdd NO2X1_5/B EN2X1_2/0 EN2X1_2/A EN2X1 MNA2X0_15 gnd vdd NO2X1_5/B EN2X1_2/0 ND5X4_1/0 INX0_9/A 001X10_7/0 NA22X0 DFF0X4_6 gnd vdd NA2X0_15/B (ND2X15_2/0 ND5X4_1/0 INX0_9/0 00121X0 MNA2X0_15 gnd vdd NA3X0_8/C ND3X1_1/0 NA201 NM2X0_16 gnd vdd NA3X0_8/C ND3X4_2/C EN2X1_4/0 ND3X1_1/0 A031X1_ A0031X1_1 gnd vdd NA3X0_8/C ND3X4_2/C EN2X1_4/0 ND2X2_3/A NU21X1 MD2CFA93_0 0.0 vdd gnd MDECA93 MN2X0_15 gvd gnd NN3X4_2/C CA031X1_1/0 ND21X1_4/0 ND3X12_1 A0331X1_1 gnd vdd NA3X0_8/C ND3X4_2/C EN2X1_4/0 ND2X2_3/A NU21X1 MD2FF0X4_4 EUX2_7/0 Vdd gnd MD2KA_2/C EN2X1_4/0 ND2X2_3/A NU21X1 MD2FF0X4_6 EUX2_7/0 Vdd gnd AD3X4_2/C EN2X1_4/0 ND2X2_3/A NU21X1 MD2FF0X4_6 EUX2_7/0 Vdd gnd AD32X1_4/0 INX0_10/A DFF0X4 HVDF0X4_6 EUX2_7/0 Vdd gnd AD32X1_4/0 INX0_10/A DF		LVS Manager
<pre>subckt frequency divider vdd gnd in N&lt;0&gt; N&lt;1&gt; N&lt;2&gt; N&lt;3&gt; N&lt;4&gt; N&lt;5&gt; reset out w n 1073741817_n1073741817# * vdd XDFF0X4 5 BUX2_7/0 vdd gnd NA22X0 3/0 INX0 9/A DFF0X4 XEN2X1_2 gnd vdd NA22X0 3/0 BUX2_4/0 N02X12_7/A EN2X1 XNA22X0_3 gnd vdd NA22X0_3/0 BUX2_4/0 N02X2_17/0 NA22x0_17/0 NA22X0 XDECAP3_0_1_0 vdd gnd DECAP3 XNA22X0_18 gnd vdd NA2X0_18/0 N02X12_17/0 NA2X0_11/0 NA22X0 XNA220_18 gnd vdd NA2X0_18/0 N02X12_17/0 NA2X0_10 NX0_9/0 0N21X0 XNA220_15 gnd vdd NA2X0_18/0 N02X12_17/0 NA2X0_10 NX0_9/0 0N21X0 XNA220_15 gnd vdd NA2X0_16/0 N02X12_10 NX0_9/0 ON21X0 XNA220_16 gnd vdd NA2X0_16/0 N02X12_10 NX0_9/0 NA2X0_ XNA220_16 gnd vdd NA3X0_8/A NO121X1_10 NA2X0_ XNA220_12 gnd vdd NA3X0_8/A NU21X1_10 NA2X0_ XNA220_13 gnd vdd NA3X0_8/A NU21X1_2X XNA221_1 gnd vdd NA3X0_8/C NO3X4_27C A031X1_1/0 A031X1_1/0 A031X1_ XDECAP3_0_0 vdd gnd DECAP3 XMU21X1_4 vdd gnd N03X4_27C A031X1_1/0 M02X2_3/A MU21X1_ XDFF0X4_2 BUX2_6/0 vdd gnd MU21X1_5/0 N03X4_27C DFF0X4 XMU21X1_5 vdd gnd N03X4_27C A031X1_1/0 M021X1_5/0 BUX2_2/0 MU21X1_ XDFF0X4_2 BUX2_6/0 vdd gnd MU21X1_5/0 BUX2_2/0 MU21X1_ XMU21X1_5 vdd gnd N1NN_7/0 MU21X1_5/0 BUX2_2/0 MU21X1_ XMU21X1_5 vdd gnd N1NN_7/0 MU21X1_4/0 MU21X1_5/0 BUX2_2/0 MU21X1_ XMU21X1_5 vdd gnd N1NN_7/0 MU21X1_5/0 BUX2_2/0 MU21X1_ XMX0_7 gnd vdd N03X4_27C A031X1_1/0 MU21X1_5/0 BUX2_2/0 MU21X1_3/ XMX0_7 gnd vdd N03X4_27C A031X1_1/0 MU21X1_5/0 BUX2_2/0 MU21X1_ XMX0_7 gnd vdd N03X4_27C A031X1_1/0 MU21X1_5/0 BUX2_2/0 MU21X1_ XMX0_7 gnd vdd N03X4_27C A031X1_1/0 XM34_27/0 HU21X1_4/0 MU21X1_5/0 BUX2_2/0 MU21X1_3/ XMX0_7 gnd vdd N03X4_27C A031X1_1/0 MU21X1_5/0 BUX2_2/0 MU21X1_X1 XMX0_7 gnd vdd N03X4_27C A031X1_1/0 XM22X0_70 XMX0_70 XM22X0_70</pre>	User: agomezs2	
1073741817_n1073741817# + vdd XDFFQX4 5 BUX2_7/Q vdd gnd NA22X0_3/Q INX0_9/A DFFQX4 KENZX1_2 gnd vdd NA2ZX0_3/Q BUX2_12/A ENZX1 XNA2ZQ 10 vdd gnd DECAP3 XNA2XQ 15 gnd vdd NA2X0_18/Q AND5X4_1/Q INX0_9/Q ON21X0 XNA2XQ 15 gnd vdd NA2X0_18/Q ND2X1_2/Q NA2X0_17/Q NA22X0 XNA2XQ 15 gnd vdd NA2X0_16/B ON21X1_2/Q N-3> ÑA2X0 XNA2XQ 15 gnd vdd NA2X0_16/B ON21X1_2/Q N-3> ÑA2X0 XNA2XQ 15 gnd vdd NA2X0_16/B ON21X1_2/Q N-3> ÑA2X0 XNA2XQ 16 gnd vdd NA2X0_16/B ON21X1_2/Q N-3> ÑA2X0 XNA2XQ 16 gnd vdd NA2X0_16/B ON21X1_2/Q N-3> ÑA2X0 XNA2X0_16 gnd vdd NA3X0_8/C N03X4_2/A INX0_8/A DFFQX4 XNDFQX4_4 BUX2_7/Q vdd gnd DFFQX4_4/D INX0_8/A DFFQX4 XN0211X2_2 gnd vdd NA3X0_8/C N03X4_2/A EN2X1 XOSIX1_1 gnd vdd N03X4_2/C EN2X1_4/Q 0A31X1_1/Q A031X1 XDECAP3_0_0 0 vdd gnd DECAP3 XMU21X1_5 vdd gnd INX0_7/Q MU21X1_5/Q BUX2_2/Q MU21X1 XDFFQX4_2 BUX2_6/Q vdd gnd MU21X1_5/Q N03X4_2/C DFFQX4 XMU21X1_5 vdd gnd INX0_7/Q MU21X1_5/Q BUX2_2/Q MU21X1 XDFCQX4_2 BUX2_6/Q vdd gnd NX4_2/C LOFFQX4 XMU21X1_5 vdd gnd INX0_7/Q MU21X1_5/Q BUX2_2/Q MU21X1 XDFFQX4_2 BUX2_6/Q vdd gnd MU21X1_5/Q BUX2_2/Q MU21X1 XDFFQX4_2 BUX2_6/Q vdd gnd INX0_7/Q MU21X1_5/Q BUX2_2/Q	Project: frequency_divider_chip /home/nwaignis/design/frequency_divid	ler_chip Layout: frequency_divider_chip Verilog netlist: frequency_divider_chip
1073741817_n1073741817# + vdd XDFFQX4 5 BUX2_7/Q vdd gnd NA22X0_3/Q INX0_9/A DFFQX4 KENZX1_2 gnd vdd NA2ZX0_3/Q BUX2_12/A ENZX1 XNA2ZQ 10 vdd gnd DECAP3 XNA2XQ 15 gnd vdd NA2X0_18/Q AND5X4_1/Q INX0_9/Q ON21X0 XNA2XQ 15 gnd vdd NA2X0_18/Q ND2X1_2/Q NA2X0_17/Q NA22X0 XNA2XQ 15 gnd vdd NA2X0_16/B ON21X1_2/Q N-3> ÑA2X0 XNA2XQ 15 gnd vdd NA2X0_16/B ON21X1_2/Q N-3> ÑA2X0 XNA2XQ 15 gnd vdd NA2X0_16/B ON21X1_2/Q N-3> ÑA2X0 XNA2XQ 16 gnd vdd NA2X0_16/B ON21X1_2/Q N-3> ÑA2X0 XNA2XQ 16 gnd vdd NA2X0_16/B ON21X1_2/Q N-3> ÑA2X0 XNA2X0_16 gnd vdd NA3X0_8/C N03X4_2/A INX0_8/A DFFQX4 XNDFQX4_4 BUX2_7/Q vdd gnd DFFQX4_4/D INX0_8/A DFFQX4 XN0211X2_2 gnd vdd NA3X0_8/C N03X4_2/A EN2X1 XOSIX1_1 gnd vdd N03X4_2/C EN2X1_4/Q 0A31X1_1/Q A031X1 XDECAP3_0_0 0 vdd gnd DECAP3 XMU21X1_5 vdd gnd INX0_7/Q MU21X1_5/Q BUX2_2/Q MU21X1 XDFFQX4_2 BUX2_6/Q vdd gnd MU21X1_5/Q N03X4_2/C DFFQX4 XMU21X1_5 vdd gnd INX0_7/Q MU21X1_5/Q BUX2_2/Q MU21X1 XDFCQX4_2 BUX2_6/Q vdd gnd NX4_2/C LOFFQX4 XMU21X1_5 vdd gnd INX0_7/Q MU21X1_5/Q BUX2_2/Q MU21X1 XDFFQX4_2 BUX2_6/Q vdd gnd MU21X1_5/Q BUX2_2/Q MU21X1 XDFFQX4_2 BUX2_6/Q vdd gnd INX0_7/Q MU21X1_5/Q BUX2_2/Q		
XDFFQX4 -5 BUX2_7/Q vdd gnd NA22X0_3/Q INX0_9/A DFFQX4XENXX1 2 gnd vdd N02X1 5/B ENXX1 2/Q ENXX1_2/A ENXX1XMA2XZ0_3 gnd vdd NA22X0_3/Q BUX2_4/Q 0N21X0_7/Q NA2X0_17/Q NA22X0XDECAP3_0_1_0 vdd gnd DECAP3XON21X0 7 gnd vdd NA2X0_18/Q NO2X2_3/A AND3X1_1/Q INX0_9/Q 0N21X0XNA2X0_18 gnd vdd NA2X0_18/Q NO2X2_3/A AND3X1_1/Q NA2X0XNA2X0_15 gnd vdd NA2X0_16/B ON2X12_1/Q NA2X0XNA2X0_16 gnd vdd DFFQX4_4/D NA2X0_2/Q NA2X0XNA2X0_12 gnd vdd NA2X0_16/B ON2X12_2/Q NA2X0XNA2X0_12 gnd vdd NA3X0_2/C EN2X1_2/Q NA2X0XN0211X2_2 gnd vdd NA3X0_2/C EN2X1_4/Q NO3X4_2/A EN2X1XN0211X2_2 gnd vdd NA3X0_8/C EN2X1_4/Q NO3X4_2/A EN2X1XN021X1_2 vdd gnd DFFQX4_4/D NA3X0_8/C EN2X1_4/Q A031X1_1/Q A031X1XN021X1_4 gnd vdd NA3X0_8/A N-1> NA3X0_8/C EN2X1_4/Q A031X1_1/Q A031X1XDFFQX4_2 BUX2_6/Q vdd gnd DECAP3XMU21X1_5 vdd gnd MU21X1_5/Q NU21X1_4/Q MU21X1_5/Q BUX2_2/Q MU21X1XINX07 7 gnd vdd NXINX07 7 gnd vdd N <td>1073741817_n1073741817#</td> <td></td>	1073741817_n1073741817#	
XNA22X0 3 gnd vdd NA22X0 3/0 BUXZ_4/0 0N21X0_7/0 NA2X0_17/0 NA2X0input real VDD3V3,XDECAP3 0_1 0 vdd gnd DECAP3input real VDD3V3,XNA2X0_18 gnd vdd NA2X0 18/0 NO2X2_3/A AND3X1_1/0 NA2X0input real VDD1V8,XNA2X0_16 gnd vdd NA2X0_16/B 0N21X1_2/0 N42X0_16/B NA2X0input real GND,XNA2X0_16 gnd vdd DFQX4_4/D INX0_8/A DEFQX4input real GND,XNA2X0_12 gnd vdd NA3X0_8/C N03X4_2/A INX0_8/A DEFQX4input real GND,XN0211X2_2 gnd vdd NA3X0_8/C N03X4_2/A INX0_8/A N0211X2input reset,XEN2X1_4 gnd vdd NA3X0_8/C N03X4_2/A EN2X1input reset,XN021X1_4 od gnd DECAP3input I/Q A031X1XMU21X1_4 vdd gnd N03X4_2/C CA031X1_1/0 N03X4_2/C DEFQX4input real VDD3V3;XMU21X1_4 vdd gnd N03X4_2/C A031X1_1/0 M021X1_5/0 BUX2_2/0 MU21X1wire real VDD3V3;XMU21X1_7 gnd vdd Ninx0_7/0 MU21X1_5/0 BUX2_2/0 MU21X1wire real VDD3V3;		
XDECAP3_0_1_0 vdd gnd DECAP3ImplementationXDECAP3_0_10 vdd gnd DECAP3ImplementationXD21X0_7 gnd vdd N021X0_7/0 NA2X0Is/0 AND5X4 1/0 INX0_9/0 ON21X0XNA2X0_18 gnd vdd NA2X0_18/0 N02X2_3/A AND3X1_1/0 NA2X0input real GND,XNA2X0_16 gnd vdd N2X0_16/B ON21X1_2/0 N<3> NA2X0input real GND,XNA2X0_16 gnd vdd DFF0X4_4/D INX0_8/A DFF0X4input real GND,XN021X2_2 gnd vdd NA3X0_8/C N03X4_2/A INX0_8/A DFF0X4input reset,XN021X2_2 gnd vdd NA3X0_8/C N03X4_2/A INX0_8/A N0211X2input reset,XEN2X1_4 gnd vdd NA3X0_8/C N03X4_2/A EN2X1output outXDECAP3_0_0_0 vdd gnd DECAP3N03X4_2/C EN2X1_4/0 N03X4_2/C DFF0X4XMU2IX1_4 vdd gnd N03X4_2/C A031X1_1/0 MU2IX1_4/0 N02X2_3/A MU2IX1input real VDD3V3;XMU2IX1_5 vdd gnd INX0_7/0 MU2IX1_5/0 BUX2_2/0 MU2IX1wire real VDD3V3;XINX0_7 gnd vdd Nvd>N		
X0N21X0_7_gnd vdd 0N21X0_7/0 NA2X0_18/0 AND5X4_1/0 INX0_9/0 0N21X0Input real VDDIV8,XMA2X0_18 gnd vdd NA2X0_18/0 N02X2_3/A AND3X1_T/0 NA2X0input real GND,XMA2X0_15 gnd vdd NA2X0_16/B 0N21X1_2/0 N<3> NA2X0input real GND,XMA2X0_16 gnd vdd NA2X0_2/0 NA2X0input real GND,XM2X0_12 gnd vdd NA3X0_8/C N03X4_2/A INX0_8/A DFF0X4input reset,XN021IX2_2 gnd vdd NA3X0_8/C N03X4_2/A INX0_8/A N021IX2input reset,XN021IX1_4 gnd vdd N03X4_2/C EN2X1_4/0 N03X4_Z/A EN2X1output outXDECAP3_0_0_0 vdd gnd DECAP3NO3X4_2/C A031X1_1/0 M021X1_4/0 N03X4_2/C DFF0X4XMU2IX1_4 vdd gnd N03X4_2/C A031X1_1/0 MU2IX1_4/0 N02X2_3/A MU2IX1wire real VDD3V3;XMU2IX1_5 vdd gnd N1X0_7/0 INX0_7/0 INX0_BUX2_6/0 MU2IX1_5/0 BUX2_2/0 MU2IX1		
XNA2X0_15 gnd vdd NA2X0_16/B 0N21X1_2/0 N<3> NA2X0       input in,         XNA2X0_16 gnd vdd DFFQX4_4/D NA22X0_2/0 NA2X0_16/B NA2X0       input in,         XDFFQX4_4 BUX2_7/0 vdd gnd DFFQX4_4/D INX0_8/A DFFQX4       input is,         XN0211X2_2 gnd vdd NA3X0_8/C N03X4_2/A INX0_8/A N0211X2       input is,         XN031X1_1 gnd vdd N03X4_2/C EN2X1_4/Q N03X4_2/A EN2X1       input reset,         XA031X1_1 gnd vdd NA3X0_8/A N<1> NA3X0_8/C EN2X1_4/Q A031X1_1/Q A031X1       input reset,         XDECAP3_0_0_0 vdd gnd DECAP3       vdd gnd N03X4_2/C A031X1_1/Q N02X2_3/A MU2IX1         XDFFQX4_2 BUX2_6/Q vdd gnd MU2IX1_5/Q N03X4_2/C DFFQX4       wire real VDD3V3;         XMU2IX1_5 vdd gnd NNX0_7/Q INX0       MU2IX1_5/Q BUX2_2/Q MU2IX1		그는 것 같은 것 같
<pre>XNA2X0_16 gnd vdd DFFQX4_4/D NA22X0_2/Q NA2X0_16/B NA2X0 XDFFQX4_4 BUX2_7/Q vdd gnd DFFQX4_4/D INX0_8/A DFFQX4 XN02I1X2_2 gnd vdd NA3X0_8/C N03X4_2/A INX0_8/A N02I1X2 XEN2X1_4 gnd vdd N03X4_2/C EN2X1_4/Q N03X4_2/A EN2X1 XA031X1_1 gnd vdd NA3X0_8/A N&lt;1&gt; NA3X0_8/C EN2X1_4/Q A031X1_1/Q A031X1 XDECAP3_0_0_0 vdd gnd DECAP3 XMU2IX1_4 vdd gnd N03X4_2/C A031X1_1/Q N02X2_3/A MU2IX1 XDFFQX4_2 BUX2_6/Q vdd gnd MU2IX1_5/Q N03X4_2/C DFFQX4 XMU2IX1_5 vdd gnd INX0_7/Q MU2IX1_4/Q MU2IX1_5/Q BUX2_2/Q MU2IX1 XINX0_7 gnd vdd N&lt;1&gt; INX0_7/Q INX0</pre>		input real GND,
XDFFQX4 4 BUX2_7/Q vdd gnd DFFQX4 4/D INX0 8/A DFFQX4         XN02I1X2_2 gnd vdd NA3X0 8/C N03X4_2/A INX0 8/A N02I1X2         XEN2X1 4 gnd vdd N03X4_2/C EN2X1_4/Q N03X4_2/A EN2X1         XA031X1_1 gnd vdd NA3X0 8/A N<1> NA3X0_8/C EN2X1_4/Q A031X1_1/Q A031X1         XDECAP3_0_0_0 vdd gnd DECAP3         XMU2IX1_4 vdd gnd N03X4_2/C A031X1_1/Q MU2IX1_4/Q N02X2_3/A MU2IX1         XDFFQX4_2 BUX2_6/Q vdd gnd MU2IX1_5/Q N03X4_2/C DFFQX4         XINX0_7 gnd vdd N<1> INX0_7/Q MU2IX1_4/Q MU2IX1_5/Q BUX2_2/Q MU2IX1		input in,
XNO2IIX2_2 gnd vdd NA3X0_8/C NO3X4_2/A INX0_8/A NO2IIX2 XEN2X1 4 gnd vdd NA3X0_8/C EN2X1_4/Q NO3X4_2/A EN2X1 XAO3IXI 1 gnd vdd NA3X0_8/A N<1> NA3X0_8/C EN2X1_4/Q AO3IX1_1/Q AO3IX1 XDECAP3_0_0_0 vdd gnd DECAP3 XMU2IX1_4 vdd gnd NO3X4_2/C AO3IX1_1/Q MU2IX1_4/Q NO2X2_3/A MU2IX1 XDFFQX4_2 BUX2_6/Q vdd gnd MU2IX1_5/Q NO3X4_2/C DFFQX4 XMU2IX1_5 vdd gnd INX0_7/Q MU2IX1_4/Q MU2IX1_5/Q BUX2_2/Q MU2IX1 XINX0_7 gnd vdd N<1> INX0_7/Q INX0 XMU2IX1_5 vdd gnd VO3X4_2/C DFFQX4		input [5:0] N,
<pre>XEN2X1_4 gnd vdd N03X4_2/C EN2X1_4/Q N03X4_2/A EN2X1 XA031XI_1 gnd vdd NA3X0_8/A N&lt;1&gt; NA3X0_8/C EN2X1_4/Q A031X1_1/Q A031X1 XDECAP3_0_0_0 vdd gnd DECAP3 XMU2IX1_4 vdd gnd N03X4_2/C A031X1_1/Q MU2IX1_4/Q N02X2_3/A MU2IX1 XDFFQX4_2 BUX2_6/Q vdd gnd MU2IX1_5/Q N03X4_2/C DFFQX4 XMU2IX1_5 vdd gnd INX0_7/Q MU2IX1_4/Q MU2IX1_5/Q BUX2_2/Q MU2IX1 XINX0_7 gnd vdd N&lt;1&gt; INX0_7/Q INX0</pre>		input reset.
XAU3IXI_1 gnd Vdd NA3X0 8/A N<1> NA3X0 8/C EN2X1_4/Q AU3IXI_1/Q AU3IXI XDECAP3_0_0_0 vdd gnd DECAP3 XMU2IX1_4 vdd gnd N03X4_2/C A03IX1_1/Q MU2IX1_4/Q N02X2_3/A MU2IX1 XDFFQX4_2 BUX2_6/Q vdd gnd MU2IX1_5/Q N03X4_2/C DFFQX4 XMU2IX1_5 vdd gnd INX0_7/Q MU2IX1_4/Q MU2IX1_5/Q BUX2_2/Q MU2IX1 XINX0_7 gnd vdd N<1> INX0_7/Q INX0 XMU2IX1_5 vdd gnd Vdd N<1> INX0_7/Q INX0	XEN2X1_4 gnd vdd N03X4_27C EN2X1_47Q N03X4_27A EN2X1	
XMU2IXI_4 vdd gnd N03X4_2/C A031X1_1/Q MU2IX1_4/Q N02X2_3/A MU2IX1 XDFFQX4_2 BUX2_6/Q vdd gnd MU2IX1_5/Q N03X4_2/C DFFQX4 XMU2IX1_5 vdd gnd INX0_7/Q MU2IX1_4/Q MU2IX1_5/Q BUX2_2/Q MU2IX1 XINX0_7 gnd vdd N<1> INX0_7/Q INX0		
XDFFQX4_2 BUX2_6/Q vdd gnd MU2IX1_5/Q NO3X4_2/C DFFQX4 XMU2IX1_5 vdd gnd INX0_7/Q MU2IX1_4/Q MU2IX1_5/Q BUX2_2/Q MU2IX1 XINX0_7 gnd vdd N<1> INX0_7/Q INX0		
XMU2IX1_5 vdd gnd INX0_7/Q MU2IX1_4/Q MU2IX1_5/Q BUX2_2/Q MU2IX1 XINX0_7 gnd vdd N<1> INX0_7/Q INX0	XDFF0X4 = 2 BUX2 6/0 vdd and MU2IX1 5/0 N03X4 2/C DFF0X4	
xDFFQX4_6 BUX2_7/Q vdd gnd A032X1_4/Q INX0_10/A DFFQX4	XINX0_7 gnd vdd N<1> INX0_7/Q INX0	이는 것 같은 것 같
	KDFFQX4_6 BUX2_7/Q vdd gnd A032X1_4/Q INX0_10/A DFFQX4	wire real GND;

#### SUMMARY

- Full backend and integration flow for a small RTL design in Efabless platform
- No cost, available to everyone
- Streamlined process steps. It took less than 3h (!)
  - Physical Implementation  $\sim$  1h
  - Top level integration ~ 2h
- IP catalog available to provide auxiliary block for your design > Rapid prototyping of new IP

VSDOpen Conference 2018

# VSDOpen Conference 2018

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Q & A