PLACEMENT & ROUTING OF DIGITAL CORE IC TO PADS USING CLOUD BASED EDA TOOL.

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Design of 6 bit Frequency divider chip using Open source tools

ACKNOWLEDGMENTS

- Tim Edwards *Open circuit design Magic Tool*
- Kunal Ghosh *VSD corp :*
- Clifford Wolf *Yosys Synthesis tool*
- *Efabless.com*

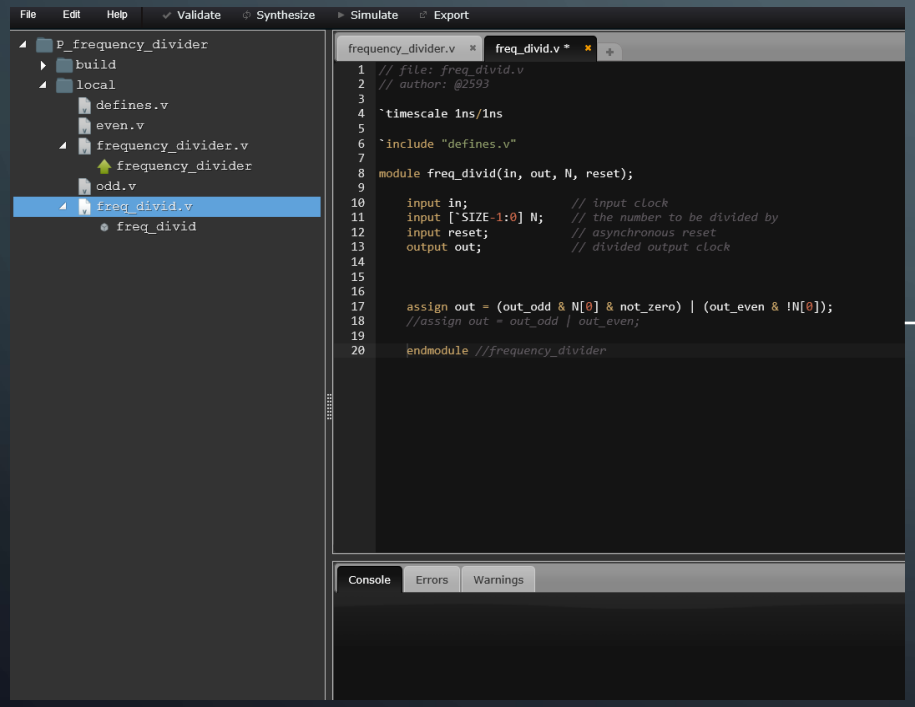
ABSTRACT

- Process Design flow of Frequency divider chip using open source tools.
- Design of complete chip in Cloud based eda tool.
- Front end tool using CloudV tool.
- Backend design of compiled netlist in OpenGalaxy tool.
- Placement & routing of synthesized core chip to I/O pads followed by addition of substrate and antenna tie down.

INTEGRATED OPEN SOURCE CLOUD BASED EDA PLATFORM

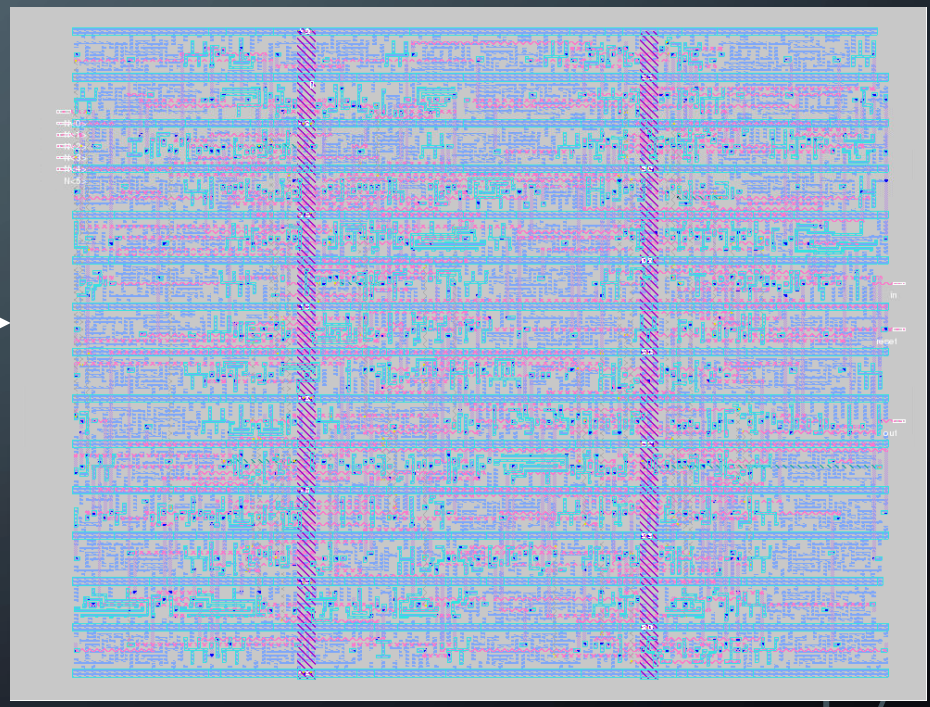
- Use of one platform consisting of various eda tools embedded into single platform instead of multiple softwares.
- A complete chip can be designed in systematic way from code to layout.
- Errors can be minimised or corrected at every stage interactively.
- Flexible & Robust.
- Works in real time.

FROM VERILOG CODE TO COMPLETE CHIP

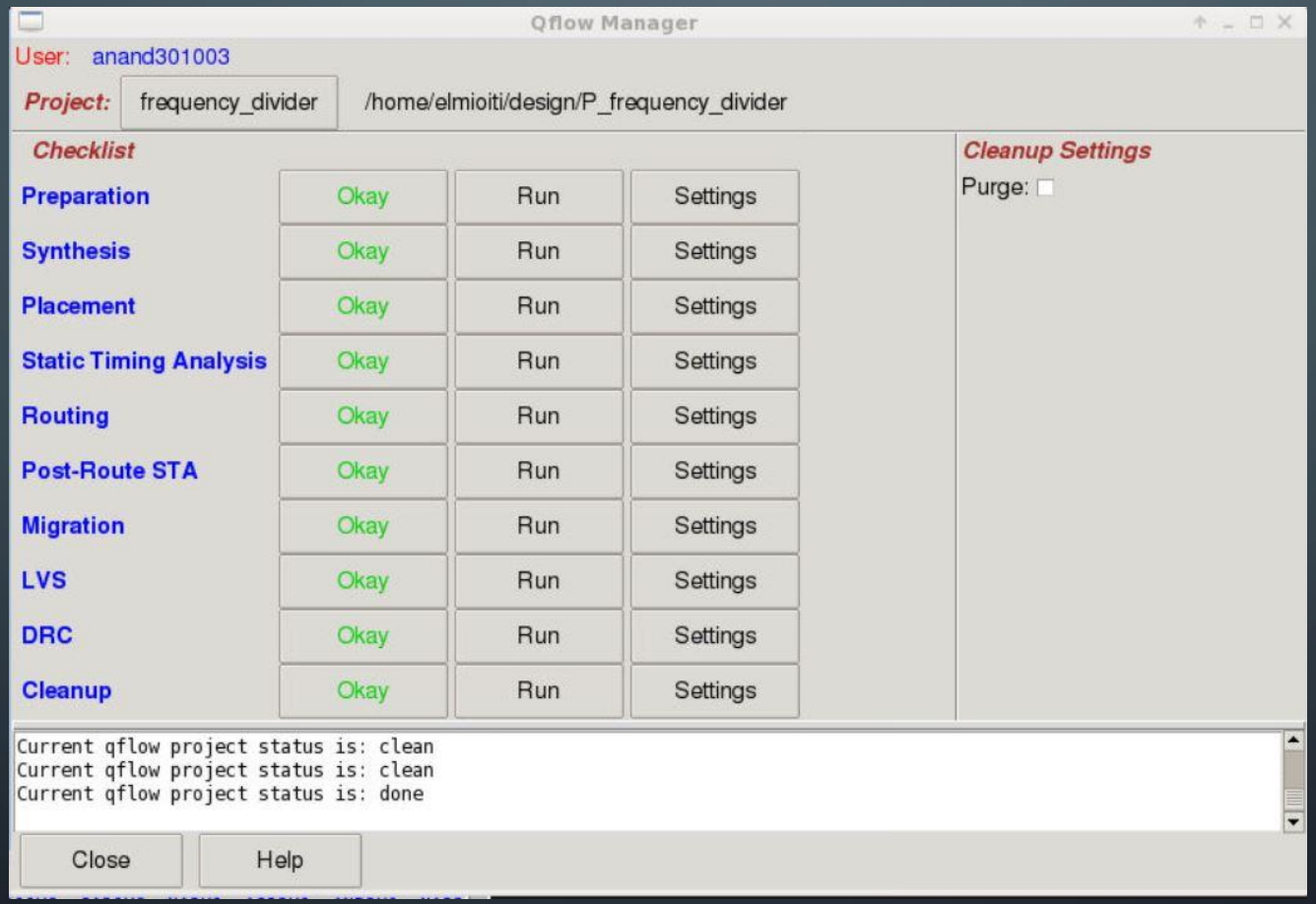


Automated configurable eda tool

Embedded into one platform



DIGITAL SYNTHESIS FLOW



REPORTS & SIMULATIONS

- Synthesis report – statistics containing no. of cells , wires inside core chip.
- Placement – User can configure the orientation of Pins in Arrange dialog box. Placement of cells are carried out in real time using Simulated annealing algorithm. Graphical view of arrangement is possible here.
- Static timing analysis: timing analysis of each & every flop is obtained and the number of paths analysed is encapsulated in a single report file.
- Routing stage: Uses global routing procedure for connections between cells. User can configure the no.of layers as min or max.
- Post STA: timing analysis is obtained but with improvement in max clock frequency.
- Migration , LVS is carried out & their reports are generated.

Synthesis reports:

```
Running yosys for verilog parsing and synthesis
yosys  -s frequency_divider.ys

 /----------------------------------------------------------------------------\
 |                                                                            |
 |  yosys -- Yosys Open SYnthesis Suite                                       |
 |                                                                            |
 |  Copyright (C) 2012 - 2016  Clifford Wolf <clifford@clifford.at>           |
 |                                                                            |
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 |                                                                            |
 \----------------------------------------------------------------------------/

 Yosys 0.6+138 (git sha1 7cddab0, gcc 4.7.4 -fPIC -Os)


-- Executing script file `frequency_divider.ys' --

1. Executing Liberty frontend.
Imported 923 cell types from liberty file.

2. Executing Verilog-2005 frontend.
Parsing Verilog input from `/home/elmioiti/design/P_frequency_divider/qflow/source/frequency_divider.v' to
AST representation.
Generating RTLIL representation for module `\frequency_divider'.
Successfully finished Verilog frontend.

3. Executing SYNTH pass.

3.1. Executing HIERARCHY pass (managing design hierarchy).

3.1.1. Analyzing design hierarchy..
Top module:  \frequency_divider

3.1.2. Analyzing design hierarchy..
Top module:  \frequency_divider
```
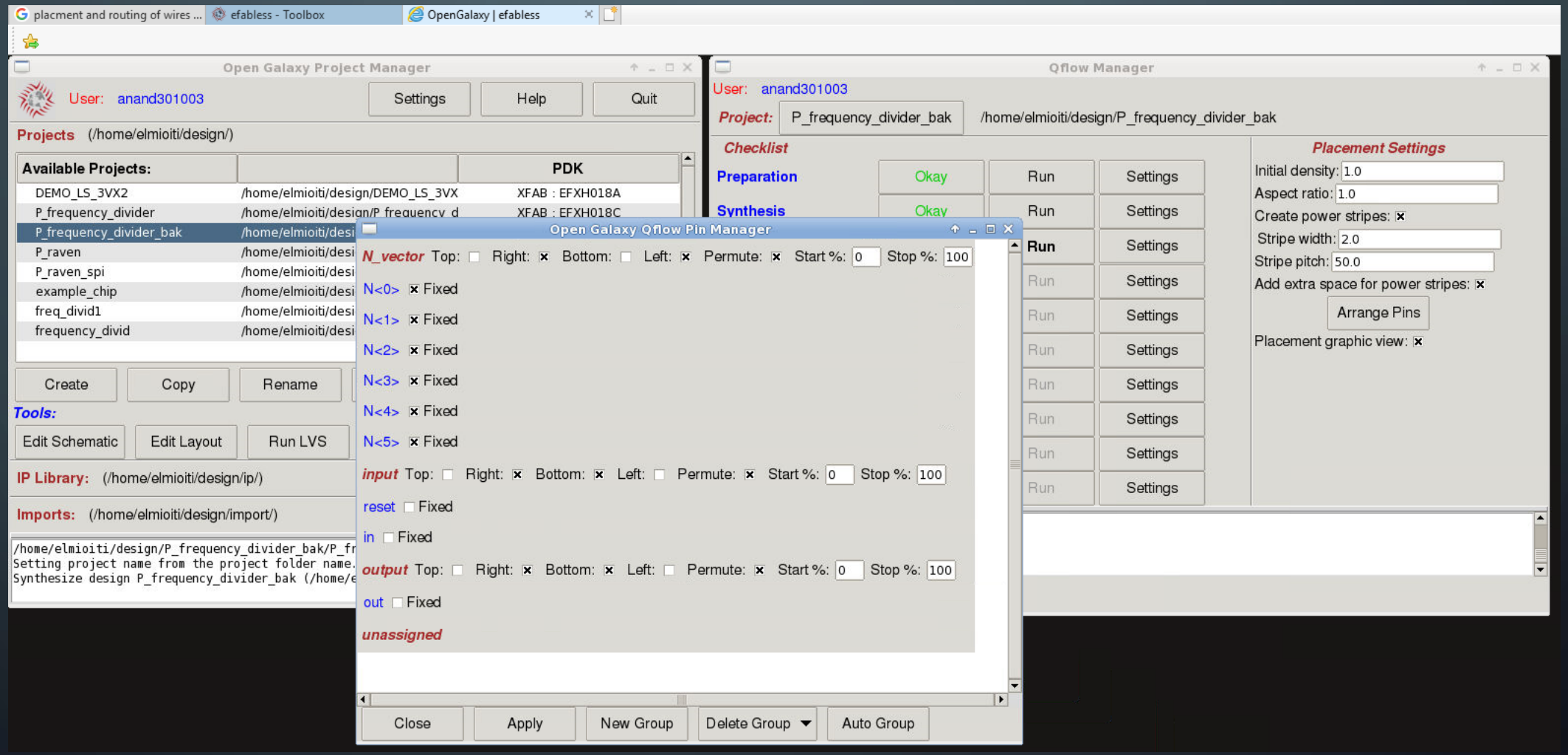
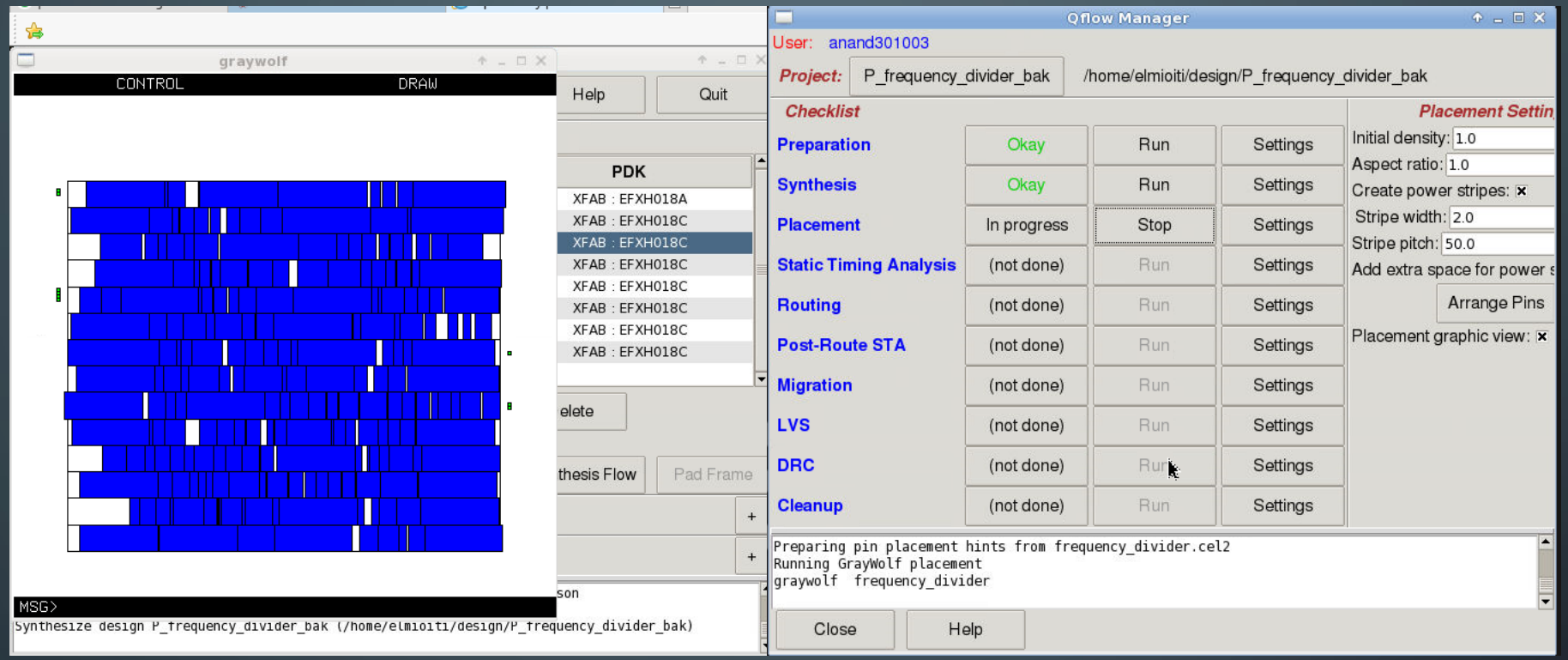

/home/elmioiti/design/P_frequency_divider_bak/qflow/log/synth.log

```
3.22.2. Analyzing design hierarchy..
Top module:  \frequency_divider
Removed 0 unused modules.

3.23. Printing statistics.

=== frequency_divider ===

   Number of wires:                184
   Number of wire bits:            234
   Number of public wires:         184
   Number of public wire bits:     234
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
   Number of cells:                226
     AN21X0                          5
     AN31X0                          2
     AN32X0                          1
     AND2X0                          3
     AND3X0                          4
     AND4X0                          2
     AND5X0                          1
     AO211X0                         1
     AO22X0                          2
     AO31X0                          2
     AO32X0                          4
     DFFQX0                         13
     DFRQX0                         13
     DFRRQX0                         6
     DFRSQX0                         2
     EN2X0                           5
     EO2X0                           5
     INX0                           21
     MU2IX0                          8
     NA22X0                          3
     NA2I1X0                         8
     NA2X0                          26
     NA3I1X0                         4
     NA3I2X0                         2
     NA3X0                          19
     NO2I1X0                         3
     NO2X0                          27
     NO3I1X0                         2
     NO3I2X0                         1
     NO3X0                           7
     NO4X0                           2
     OA21X0                          2
     ON21X0                         15
     ON31X0                          3
     OR2X0                           1
     OR5X0                           1

3.24. Executing CHECK pass (checking for obvious problems).
checking module frequency_divider..
found and reported 0 problems.

4. Executing DFFLIBMAP pass (mapping DFF cells to sequential cells from liberty file).
  cell DFFQX0 (noninv, pins=3, area=49.19) is a direct match for cell type $_DFF_N_.
  cell DFRQX0 (noninv, pins=3, area=49.19) is a direct match for cell type $_DFF_P_.
```

Config of orientation of I/O pins at core cell




graywolf
CONTROL
DRAW
MSG>
Synthesize design P_frequency_divider_bak (/home/elmioiti/design/P_frequency_divider_bak)
Help
Quit
PDK
XFAB : EFXH018A
XFAB : EFXH018C
XFAB : EFXH018C
XFAB : EFXH018C
XFAB : EFXH018C
XFAB : EFXH018C
XFAB : EFXH018C
XFAB : EFXH018C
elete
thesis Flow
Pad Frame
Qflow Manager
User: anand301003
Project: P_frequency_divider_bak
/home/elmioiti/design/P_frequency_divider_bak
Checklist
Preparation Okay Run Settings
Synthesis Okay Run Settings
Placement In progress Stop Settings
Static Timing Analysis (not done) Run Settings
Routing (not done) Run Settings
Post-Route STA (not done) Run Settings
Migration (not done) Run Settings
LVS (not done) Run Settings
DRC (not done) Run Settings
Cleanup (not done) Run Settings
Placement Settin
Initial density: 1.0
Aspect ratio: 1.0
Create power stripes:
Stripe width: 2.0
Stripe pitch: 50.0
Add extra space for power s
Arrange Pins
Placement graphic view:
Preparing pin placement hints from frequency_divider.cel2
Running GrayWolf placement
graywolf frequency_divider
Close
Help

RESULTS AND WIP

```
716.8 ps            _34__4_: NA22X0_3/Q -> DFFQX4_5/D

esign meets minimum hold timing.
----------------------------------------

Number of paths analyzed:  77

Top 20 maximum delay paths:
Path input pin N[1] to DFRRQX4_6/D delay 1333.45 ps
     0.0 ps             N[1]:              ->   OR5X4_1/E
   589.7 ps  even_0_not_zero:   OR5X4_1/Q ->  AND2X4_1/A
   795.1 ps       enable_odd:  AND2X4_1/Q ->    INX1_2/A
  1038.0 ps            _128_:    INX1_2/Q ->   NO2X1_4/B
  1228.2 ps            _145_:   NO2X1_4/Q ->  AN32X1_1/C
  1462.5 ps             _39_:  AN32X1_1/Q -> DFRRQX4_6/D

Path input pin N[1] to DFRQX4_7/D delay 1284.38 ps
     0.0 ps             N[1]:              ->   OR5X4_1/E
   589.7 ps  even_0_not_zero:   OR5X4_1/Q ->  AND2X4_1/A
   795.1 ps       enable_odd:  AND2X4_1/Q ->    INX1_2/A
  1038.0 ps            _128_:    INX1_2/Q ->   NO2X2_6/A
  1296.6 ps             _99_:   NO2X2_6/Q ->  OA21X0_1/B
  1817.5 ps            _100_:  OA21X0_1/Q -> AO211X0_1/C
  2528.6 ps          _35__0_: AO211X0_1/Q ->  DFRQX4_7/D

Path input pin N[1] to DFFQX4_13/D delay 1193.4 ps
```

```
low terminated normally with no errors and 0 warning[s]

unning getfillcell to determine cell to use for fill.
getfillcell.tcl frequency_divider /ef/tech/XFAB.3/EFXH018C/libs.ref/lef/D_CELLS/xh018_D_CELLS.lef DECAP
Using cell DECAP for fill
Running place2def to translate graywolf output to DEF format.
lace2def.tcl frequency_divider DECAP
Running place2def.tcl
DEF database: nanometers
Limits: xbot = -360.5 ybot = -136 xtop = 8298.5 ytop = 6696
Core values: 31.5 0 8347.5 6832
Offsets: 31.5 0
6 routing layers
113 horizontal tracks from -61.0 to 6832.0 step 61.0 (M1, M3, ...)
138 vertical tracks from -189.0 to 8505.0 step 63.0 (M2, M4, ...)
Done with place2def.tcl
Running addspacers to generate power stripes and align cell right edge
addspacers.tcl -techlef /ef/tech/XFAB.3/EFXH018C/libs.ref/techLEF/xh018_xx51_MET5_METMID.lef -stripe 2.0 50.
/ef/tech/XFAB.3/EFXH018C/libs.ref/lef/D_CELLS/xh018_D_CELLS.lef DECAP
Reading technology LEF file /ef/tech/XFAB.3/EFXH018C/libs.ref/techLEF/xh018_xx51_MET5_METMID.lef.
Reading DECAP macros from LEF file.
Reading DEF file frequency_divider.def. . .
Number of rows is 14
Longest row has width 83.475 um
addspacers:  No room for stripes, pitch reduced from 49770.0 to 34902.0.
addspacers:  Inserting 2 stripes of width 1.89 um (2.0 um requested)
  Pitch 34.902 um, offset 23.94 um
stretch:  Number of components is 264
Analysis of DEF file:
Number of components = 236
New number of components = 264
Number of rows = 14
Stripe width 1890 fits 3 VIA1_X_so at cut width 260.0 separation 260.0
Stripe width 1890 fits 3 VIA2_so at cut width 260.0 separation 260.0
Stripe width 1890 fits 3 VIA3_so at cut width 260.0 separation 260.0
Stripe width 1890 fits 3 VIA4_so at cut width 260.0 separation 260.0
Stripe width 1890 fits 2 VIATP_X_so at cut width 360.0 separation 350.0
```

STA REPORT

Design meets minimum hold timing
No.of paths analysed: 77
Max path delay : N[1] to DFRRQX4_6/D is 1333.45 ps Min path delay : DFRRQX4_5/C to DFRRQX4_5/D is 632.357ps

PLACEMENT REPORT

	User input	Practical output
Stripe width	2 µm	1.89 µm
Stripe pitch	50 µm	34.902 µm

STA log file

```
Design meets minimum hold timing.
-----------------------------------------

Number of paths analyzed:  77

Top 20 maximum delay paths:
Path input pin N[1] to DFRRQX4_6/D delay 1333.45 ps
      0.0 ps             N[1]:              ->   OR5X4_1/E
    589.7 ps  even_0_not_zero:   OR5X4_1/Q ->  AND2X4_1/A
    795.1 ps       enable_odd:  AND2X4_1/Q ->    INX1_2/A
   1038.0 ps            _128_:    INX1_2/Q ->   NO2X1_4/B
   1228.2 ps            _145_:   NO2X1_4/Q ->  AN32X1_1/C
   1462.5 ps             _39_: AN32X1_1/Q -> DFRRQX4_6/D

Path input pin N[1] to DFRQX4_7/D delay 1284.38 ps
      0.0 ps             N[1]:              ->   OR5X4_1/E
    589.7 ps  even_0_not_zero:   OR5X4_1/Q ->  AND2X4_1/A
    795.1 ps       enable_odd:  AND2X4_1/Q ->    INX1_2/A
   1038.0 ps            _128_:    INX1_2/Q ->   NO2X2_6/A
   1296.6 ps             _99_:   NO2X2_6/Q ->   OA21X0_1/B
   1817.5 ps            _100_:  OA21X0_1/Q -> AO211X0_1/C
   2528.6 ps          _35__0_: AO211X0_1/Q ->  DFRQX4_7/D

Path input pin N[1] to DFFQX4_13/D delay 1193.4 ps
```

Open Galaxy Text Report

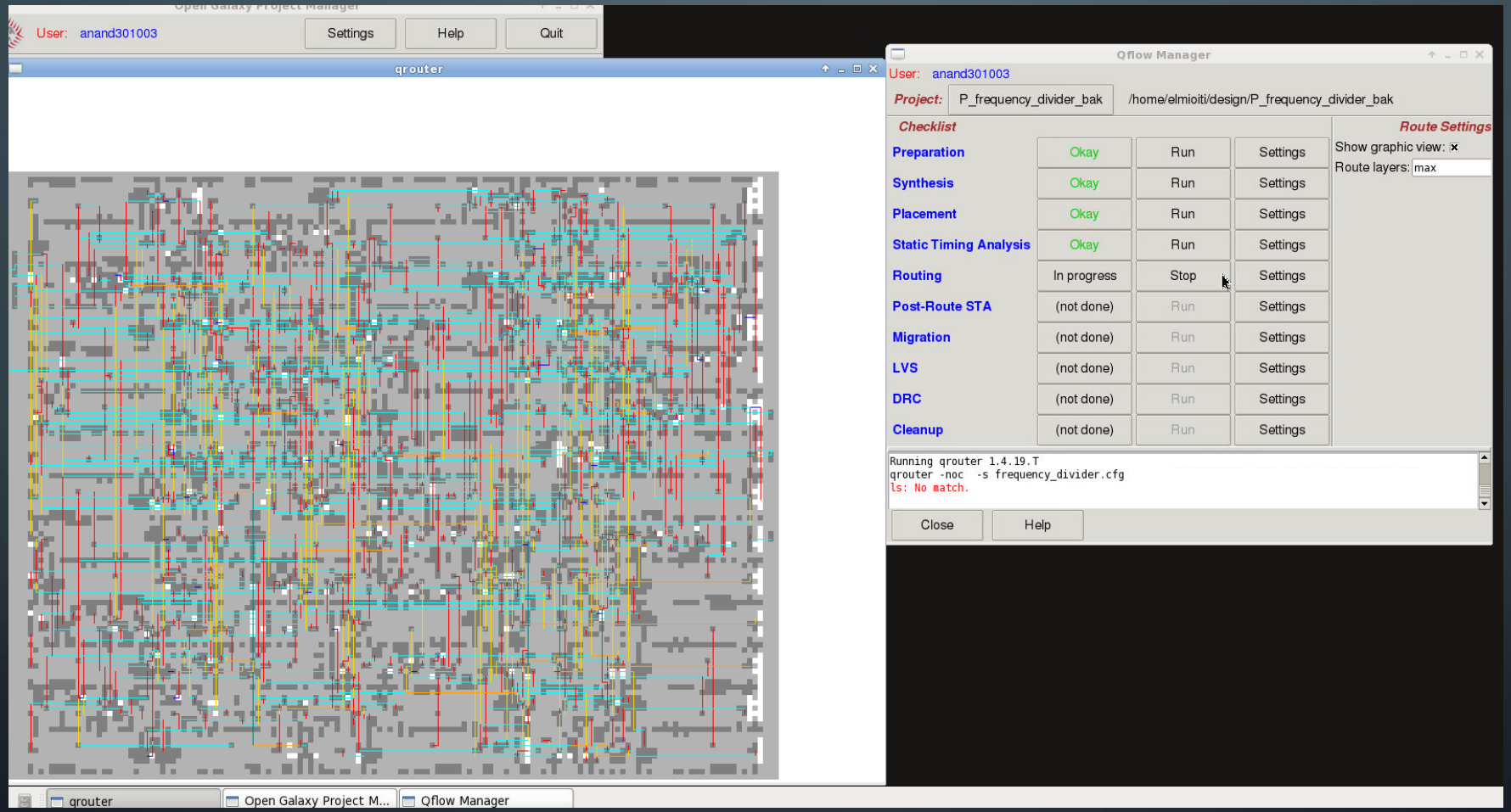
/home/elmioiti/design/P_frequency_divider_bak/qflow/log/sta.log

```
Qflow static timing analysis logfile created on Sat Aug 4 04:23:37 PDT 2018
Running vesta static timing analysis
vesta --long frequency_divider.rtlnopwr.v /ef/tech/XFAB.3/EFXH018C/libs.ref/liberty/D_CELLS/D_CELLS_LPMOS_typ_1_80V_25C.lib
-----------------------------------------
Vesta static timing analysis tool
(c) 2013-2017 Tim Edwards, Open Circuit Design
-----------------------------------------

Parsing library "D_CELLS_LPMOS_typ_1_80V_25C"
End of library at line 426120
Parsing module "frequency_divider"
Lib Read:  Processed 426121 lines.
Verilog netlist read:  Processed 248 lines.
Number of paths analyzed:  29

Top 20 maximum delay paths:
Path DFFQX4_9/CN to DFFQX4_12/D delay 2154.55 ps
      0.0 ps             in_bF_buf4:   BUX2_5/Q ->  DFFQX4_9/CN
    603.9 ps  odd_0_initial_begin_1_: DFFQX4_9/Q ->   NO2X1_6/B
    797.5 ps                  _161_:  NO2X1_6/Q ->   NA2X2_1/A
    984.4 ps                  _162_:  NA2X2_1/Q ->  ON31X0_2/C
   1314.4 ps                   _46_: ON31X0_2/Q ->  NA2X0_12/A
   1566.0 ps                   _49_: NA2X0_12/Q ->  AO32X1_3/E
   1973.9 ps                 _36__4_: AO32X1_3/Q -> DFFQX4_12/D

Path DFFQX4_11/CN to DFFQX4_13/D delay 1911.27 ps
      0.0 ps             in_bF_buf1:    BUX2_8/Q -> DFFQX4_11/CN
    614.2 ps  odd_0_initial_begin_3_: DFFQX4_11/Q ->   NO3X4_1/B
    861.3 ps                  _149_:   NO3X4_1/Q ->  AND3X4_1/A
   1137.0 ps                  _155_:  AND3X4_1/Q ->   NO2X2_3/A
   1302.5 ps                  _156_:   NO2X2_3/Q ->  AO31X0_1/A
   1823.8 ps                 _36__5_:  AO31X0_1/Q -> DFFQX4_13/D

Path DFFQX4_11/CN to DFFQX4_5/D delay 1827.87 ps
      0.0 ps             in_bF_buf1:    BUX2_8/Q -> DFFQX4_11/CN
    614.2 ps  odd_0_initial_begin_3_: DFFQX4_11/Q ->   NO3X4_1/B
    861.3 ps                  _149_:   NO3X4_1/Q ->  AND5X4_1/B
   1350.3 ps                   _83_:  AND5X4_1/Q ->  ON21X0_7/A
   1570.1 ps                   _87_:  ON21X0_7/Q ->  NA22X0_3/B
   1889.4 ps                 _34__4_:  NA22X0_3/Q ->  DFFQX4_5/D

Path DFFQX4_2/CN to DFFQX4_6/D delay 1807.52 ps
      0.0 ps            in_bF_buf2:   BUX2_7/Q -> DFFQX4_2/CN
    618.2 ps  odd_0_counter2_1_: DFFQX4_2/Q ->  NO2X1_9/B
    809.2 ps                  _77_:  NO2X1_9/Q -> NA3X0_11/C
   1072.4 ps                  _90_: NA3X0_11/Q -> ON21X0_8/B
   1392.5 ps                  _91_: ON21X0_8/Q -> AO32X1_4/C
   1878.1 ps                _34__5_: AO32X1_4/Q -> DFFQX4_6/D

Path DFFQX4_11/CN to DFFQX4_4/D delay 1789.11 ps
      0.0 ps             in_bF_buf1:    BUX2_8/Q -> DFFQX4_11/CN
    614.2 ps  odd_0_initial_begin_3_: DFFQX4_11/Q ->   NO3X4_1/B
    861.3 ps                  _149_:   NO3X4_1/Q ->  NA3X2_1/A
```

/home/elmioiti/design/P_frequency_divider_bak/qflow/log/sta.log

```
      0.0 ps            in_bF_buf2:    BUX2_7/Q ->  DFFQX4_2/CN
    618.2 ps  odd_0_counter2_1_:  DFFQX4_2/Q ->  ON21X0_5/B
    886.9 ps                  _66_:  ON21X0_5/Q -> NO2I1X0_1/AN
   1185.6 ps                  _67_: NO2I1X0_1/Q ->  NA2X0_14/B
   1424.1 ps                  _69_:  NA2X0_14/Q ->  MU2IX1_6/IN1
   1651.3 ps                  _70_:  MU2IX1_6/Q ->  MU2IX1_7/IN1
   1850.2 ps                _34__2_:  MU2IX1_7/Q ->  DFFQX4_3/D

Computed maximum clock frequency (zero slack) = 464.135 MHz
-----------------------------------------

Number of paths analyzed:  29

Top 20 minimum delay paths:
Path DFRRQX4_5/C to DFRRQX4_5/D delay 632.357 ps
      0.0 ps            in_bF_buf0:    BUX2_9/Q -> DFRRQX4_5/C
    479.7 ps  even_0_counter_5_: DFRRQX4_5/Q ->  AN31X1_1/D
    543.8 ps                  _31_:  AN31X1_1/Q ->   NO2X0_3/A
    606.1 ps                _2__5_:   NO2X0_3/Q -> DFRRQX4_5/D

Path DFRSQX4_1/C to DFRSQX4_1/D delay 667.499 ps
      0.0 ps            in_bF_buf1:    BUX2_8/Q -> DFRSQX4_1/C
    399.2 ps  even_0_counter_0_: DFRSQX4_1/Q -> NA2I1X0_2/B
    488.0 ps                  _13_: NA2I1X0_2/Q ->   NA3X0_3/B
    608.7 ps                _2__0_:   NA3X0_3/Q -> DFRSQX4_1/D

Path DFRSQX4_2/C to DFRSQX4_2/D delay 704.881 ps
      0.0 ps           in_bF_buf0:    BUX2_9/Q -> DFRSQX4_2/C
    356.5 ps  even_0_out_counter: DFRSQX4_2/Q ->  ON31X0_1/D
    469.5 ps                   _7_:  ON31X0_1/Q ->   NA2X0_2/A
    558.8 ps                   _3_:   NA2X0_2/Q -> DFRSQX4_2/D

Path DFRQX4_4/C to DFRRQX4_6/D delay 720.64 ps
      0.0 ps      in_bF_buf3:    BUX2_6/Q ->  DFRQX4_4/C
    369.7 ps  odd_0_old_N_3_:  DFRQX4_4/Q ->   NO2X2_2/B
    438.8 ps                  _136_:   NO2X2_2/Q -> NO3I1X2_2/B
    504.6 ps                  _139_: NO3I1X2_2/Q ->  AN32X1_1/B
    624.2 ps                   _39_:  AN32X1_1/Q -> DFRRQX4_6/D

Path DFRQX4_9/C to DFRQX4_9/D delay 730.154 ps
      0.0 ps           in_bF_buf3:   BUX2_6/Q -> DFRQX4_9/C
    460.9 ps  odd_0_counter_2_: DFRQX4_9/Q ->  NO2X2_7/B
    558.7 ps                  _107_:  NO2X2_7/Q ->  NO3X2_2/C
    634.5 ps                  _109_:  NO3X2_2/Q -> MU2IX1_8/IN1
    721.7 ps                _35__2_: MU2IX1_8/Q -> DFRQX4_9/D

Path DFFQX4_11/CN to DFFQX4_11/D delay 749.951 ps
      0.0 ps             in_bF_buf1:    BUX2_8/Q -> DFFQX4_11/CN
    397.7 ps  odd_0_initial_begin_3_: DFFQX4_11/Q ->   NO3X2_1/B
    482.1 ps                   _40_:   NO3X2_1/Q ->  ON21X0_3/B
    584.0 ps                   _42_:  ON21X0_3/Q ->  NA2X0_11/B
    662.7 ps                 _36__3_:  NA2X0_11/Q -> DFFQX4_11/D
```

ROUTING STAGE

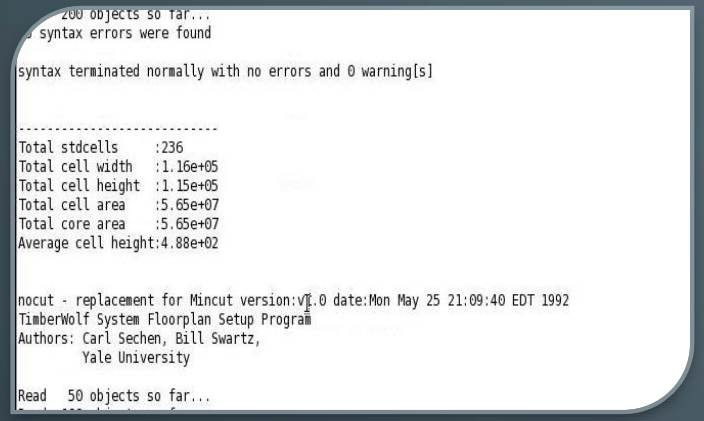


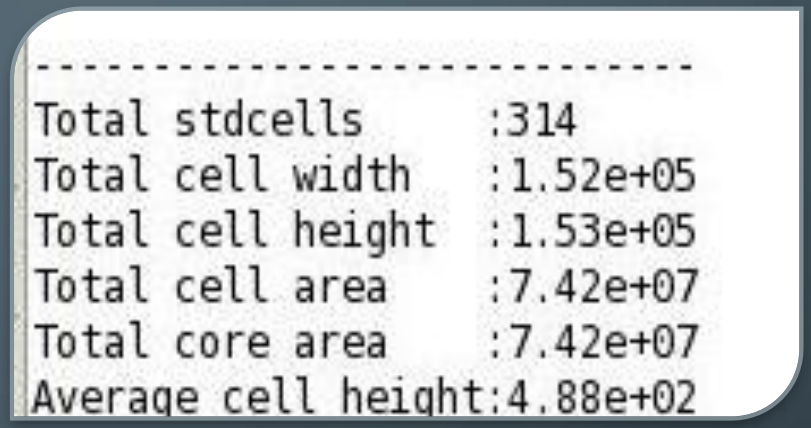
Routing reports

```
TimberWolfSC version:v6.0 date:Mon May 25 21:19:07 EDT 1992
Row-Based Placement and Global Routing Program
Authors: Carl Sechen, Kai-Win Lee, and Bill Swartz,
         Yale University
  0
  1   2   3   4   5   6   7   8   9  10  11  12  13  14  15
 16  17  18  19  20  21  22  23  24  25  26  27  28  29  30
 31  32  33  34  35  36  37  38  39  40  41  42  43  44  45
 46  47  48  49  50  51  52  53  54  55  56  57  58  59  60
 61  62  63  64  65  66  67  68  69  70  71  72  73  74  75
 76  77  78  79  80  81  82  83  84  85  86  87  88  89  90
 91  92  93  94  95  96  97  98  99 100 101 102 103 104 105
106 107 108 109 110 111 112 113 114 115 116 117 118 119 120
121 122 123 124 125 126 127 128 129 130 131 132 133 134 135
136 137 138 139 140 141 142 143 144 145 146 147 148 149 150
151 152 153 154 155 156 157 158
 block left edge is at -185
 the longest block length is 8694
 building the steiner trees
 rebuilding the steiner tree

----start doing coarse global routing ------
 ITERATION  1

  longest Row is:1   Its length is:8316
 doing feed-through pins assignment
 building the net-tree now !
 set up the global routing grids
 the starting value of tracks =   95
 tracks =  87 at attempts =  1000
 tracks =  86 at attempts =  2000
 tracks =  86 at attempts =  3000
 tracks =  86 at attempts =  4000
 tracks =  86 at attempts =  5000
 tracks =  86 at attempts =  6000
 removing redundant feed-through pins
 the connectivity of all the nets is verified

 block left edge is at -185
 the longest block length is 8694
 building the steiner trees
 rebuilding the steiner tree
```

```
syntax version:v1.1 date:Mon May 25 21:11:10 EDT 1992
TimberWolf System Syntax Checker
Authors: Carl Sechen, Kai-Win Lee, Bill Swartz,
         Dahe Chen, and Jimmy Lam
         Yale University

Read   50 objects so far...
Read  100 objects so far...
Read  150 objects so far...
Read  200 objects so far...
No syntax errors were found

syntax terminated normally with no errors and 0 warning[s]


----------------------------
Total stdcells     :236
Total cell width   :1.16e+05
Total cell height  :1.15e+05
Total cell area    :5.65e+07
Total core area    :5.65e+07
Average cell height:4.88e+02


nocut - replacement for Mincut version:v1.0 date:Mon May 25 21:09:40 EDT 1992
TimberWolf System Floorplan Setup Program
Authors: Carl Sechen, Bill Swartz,
         Yale University

Read   50 objects so far...
Read  100 objects so far...
Read  150 objects so far...
Read  200 objects so far...
Splitting frequency_divider.cel into frequency_divider.scel and frequency_divider.mcel...
        done!


nocut - replacement for Mincut terminated normally with no errors and 0 warning[s]
```

RESULTS AND WIP





attributes	N=6	N=8
Total stdcells	236	314
Total cell width	116000 nm	152000 nm
Total cell height	115000 nm	153000 nm
Total cell area	56500 µm	74200 µm
Total core area	56500 µm	74200 µm
Average cell height	488 µm	488 µm
Horizontal tracks	113	137
Vertical tracks	138	147
No. of Routing layers	6	6

Routing reports cont'd

```
----start doing coarse global routing ------
 ITERATION  1

  longest Row is:1   Its length is:8316
 doing feed-through pins assignment
 building the net-tree now !
 set up the global routing grids
 the starting value of tracks =   98
 tracks =  85 at attempts =  1000
 tracks =  85 at attempts =  2000
 tracks =  85 at attempts =  3000
 tracks =  85 at attempts =  4000
 tracks =  85 at attempts =  5000
 tracks =  85 at attempts =  6000
 removing redundant feed-through pins
 the connectivity of all the nets is verified

 block left edge is at -185
 the longest block length is 8694
 building the steiner trees
 rebuilding the steiner tree

----start doing coarse global routing ------
 ITERATION  1

  longest Row is:1   Its length is:8316
 doing feed-through pins assignment
 building the net-tree now !
 set up the global routing grids
 the starting value of tracks =  111
 tracks = 109 at attempts =  1000
 tracks = 109 at attempts =  2000
 tracks = 109 at attempts =  3000
 tracks = 109 at attempts =  4000
 tracks = 109 at attempts =  5000
 tracks = 109 at attempts =  6000
 removing redundant feed-through pins
 the connectivity of all the nets is verified


**********************************************
*ACTUAL* FINAL NUMBER OF ROUTING TRACKS: 81
**********************************************
```

```
Finished routing net _104_
Nets remaining: 47
Finished routing net _106_
Nets remaining: 46
Finished routing net _109_
Nets remaining: 45
Finished routing net _35_<2>
Nets remaining: 44
Finished routing net _110_
Nets remaining: 43
Finished routing net _112_
Nets remaining: 42
Finished routing net _113_
Nets remaining: 41
Finished routing net _35_<3>
Nets remaining: 40
Finished routing net _114_
Nets remaining: 39
Finished routing net _116_
Nets remaining: 38
Finished routing net _117_
Nets remaining: 37
Finished routing net _118_
Nets remaining: 36
Finished routing net _35_<4>
Nets remaining: 35
Finished routing net _119_
Nets remaining: 34
Finished routing net _120_
Nets remaining: 33
Finished routing net _121_
Nets remaining: 32
Finished routing net _122_
Nets remaining: 31
Finished routing net _123_
Nets remaining: 30
Finished routing net _124_
Nets remaining: 29
Finished routing net _35_<5>
Nets remaining: 28
Finished routing net _125_
Nets remaining: 27
Finished routing net _126_
Nets remaining: 26
Finished routing net _37_
Nets remaining: 25
Finished routing net _127_
Nets remaining: 24
Finished routing net _38_
Nets remaining: 23
Finished routing net _108_
Nets remaining: 22
Finished routing net out
Nets remaining: 21

---------------------------------------------
Progress: Stage 1 total routes completed: 550
Failed net routes: 20
---------------------------------------------
*** Running stage2 routing with options mask 10, effort 10
Nets remaining: 20
Nets remaining: 19
Best route of _76_ collides with net: _75_
```

```
---------------------------------------------
Progress: Stage 1 total routes completed: 550
Failed net routes: 20
---------------------------------------------
*** Running stage2 routing with options mask 10, effort 10
Nets remaining: 20
Nets remaining: 19
Best route of _76_ collides with net: _75_
Ripping up blocking net _75_
Nets remaining: 19
Best route of _34_<2> collides with net: N<2>
Ripping up blocking net N<2>
Nets remaining: 19
Nets remaining: 18
Nets remaining: 17
Best route of _54_ collides with nets: _48_ N<4>
Ripping up blocking net _48_
Ripping up blocking net N<4>
Nets remaining: 18
Nets remaining: 17
Nets remaining: 16
Best route of _142_ collides with net: _141_
Ripping up blocking net _141_
Nets remaining: 16
Best route of _31_ collides with nets: _27_ _2_<5>
Ripping up blocking net _27_
Ripping up blocking net _2_<5>
Nets remaining: 17
Nets remaining: 16
Nets remaining: 15
Best route of _95_ collides with net: _92_
Ripping up blocking net _92_
Nets remaining: 15
Best route of odd_0.counter2<4> collides with net: odd_0.counter2<1>
Ripping up blocking net odd_0.counter2<1>
Nets remaining: 15
Best route of _149_ collides with net: _148_
Ripping up blocking net _148_
Nets remaining: 15
Best route of even_0.counter<4> collides with net: even_0.counter<2>
Ripping up blocking net even_0.counter<2>
Nets remaining: 15
Best route of N<3> collides with net: N<0>
Ripping up blocking net N<0>
Nets remaining: 15
Nets remaining: 14
Nets remaining: 13
Nets remaining: 12
Best route of _75_ collides with net: in
Ripping up blocking net in
Nets remaining: 12
Nets remaining: 11
Nets remaining: 10
Nets remaining: 9
Nets remaining: 8
Nets remaining: 7
Best route of _2_<5> collides with net: _84_
Ripping up blocking net _84_
Nets remaining: 7
Nets remaining: 6
Nets remaining: 5
Nets remaining: 4
```

2nd Stage of Routing: No failed routes

```
------------------------------------------------
Progress: Stage 2 total routes completed: 637
No failed routes!
------------------------------------------------
*** Running stage3 routing with defaults, 1st round
Finished routing net N<0>
Nets remaining: 245
Finished routing net N<1>
Nets remaining: 244
Finished routing net N<4>
Nets remaining: 243
Finished routing net N<5>
Nets remaining: 242
Finished routing net N<2>
Nets remaining: 241
Failed to remove stacked via at grid point 56 66.
Failed to route net in_bF$buf4; restoring original
Finished routing net in_bF$buf3
Nets remaining: 239
Finished routing net in_bF$buf2
Nets remaining: 238
Finished routing net in_bF$buf1
Nets remaining: 237
Finished routing net in_bF$buf0
Nets remaining: 236
Finished routing net N<3>
Nets remaining: 235
Finished routing net enable_even
Nets remaining: 234
Finished routing net enable_odd
Nets remaining: 233
Finished routing net _9_
Nets remaining: 232
Finished routing net _24_
Nets remaining: 231
Finished routing net _155_
Nets remaining: 230
Finished routing net odd_0.counter2<0>
Nets remaining: 229
Finished routing net even_0.counter<2>
Nets remaining: 228
Finished routing net even_0.counter<0>
Nets remaining: 227
Finished routing net _10_
Nets remaining: 226
Finished routing net _17_
Nets remaining: 225
Finished routing net _128_
Nets remaining: 224
Finished routing net _152_
Nets remaining: 223
```

```
************************************************
*ACTUAL* FINAL NUMBER OF ROUTING TRACKS: 81
************************************************


TimberWolfSC terminated normally with no errors and 0 warning[s]


twflow terminated normally with no errors and 0 warning[s]

Running getfillcell to determine cell to use for fill.
getfillcell.tcl frequency_divider /ef/tech/XFAB.3/EFXH018C/libs.ref/lef/D_CELLS/xh018_D_CELLS.lef DECAP
Using cell DECAP for fill
Running place2def to translate graywolf output to DEF format.
place2def.tcl frequency_divider DECAP
Running place2def.tcl
DEF database: nanometers
Limits: xbot = -360.5 ybot = -136 xtop = 8298.5 ytop = 6696
Core values: 31.5 0 8347.5 6832
Offsets: 31.5 0
6 routing layers
113 horizontal tracks from -61.0 to 6832.0 step 61.0 (M1, M3, ...)
138 vertical tracks from -189.0 to 8505.0 step 63.0 (M2, M4, ...)
Done with place2def.tcl
Running addspacers to generate power stripes and align cell right edge
addspacers.tcl -techlef /ef/tech/XFAB.3/EFXH018C/libs.ref/techLEF/xh018_xx51_MET5_METMID.lef -stripe 2.0 50.
/ef/tech/XFAB.3/EFXH018C/libs.ref/lef/D_CELLS/xh018_D_CELLS.lef DECAP
Reading technology LEF file /ef/tech/XFAB.3/EFXH018C/libs.ref/techLEF/xh018_xx51_MET5_METMID.lef.
Reading DECAP macros from LEF file.
Reading DEF file frequency_divider.def. . .
Number of rows is 14
Longest row has width 83.475 um
addspacers:  No room for stripes, pitch reduced from 49770.0 to 34902.0.
addspacers:  Inserting 2 stripes of width 1.89 um (2.0 um requested)
  Pitch 34.902 um, offset 23.94 um
stretch:  Number of components is 264
Analysis of DEF file:
Number of components = 236
New number of components = 264
Number of rows = 14
Stripe width 1890 fits 3 VIA1_X_so at cut width 260.0 separation 260.0
Stripe width 1890 fits 3 VIA2_so at cut width 260.0 separation 260.0
Stripe width 1890 fits 3 VIA3_so at cut width 260.0 separation 260.0
Stripe width 1890 fits 3 VIA4_so at cut width 260.0 separation 260.0
Stripe width 1890 fits 2 VIATP_X_so at cut width 360.0 separation 350.0
Adjusting obstructions for power striping
Done with addspacers.tcl
blifanno.tcl /home/elmioiti/design/P_frequency_divider/qflow/synthesis/frequency_divider.blif frequency_divi
/home/elmioiti/design/P_frequency_divider/qflow/synthesis/frequency_divider_anno.bli
Running blifanno.tcl
```

Qrouter:

/home/elmioiti/design/P_frequency_divider_bak/qflow/log/route.log

```
Qflow route logfile created on Sat Aug 4 04:24:01 PDT 2018
qrouter -nog  -s frequency_divider.cfg
Qrouter detail maze router version 1.3.100.T
Reading LEF data from file /ef/tech/XFAB.3/EFXH018C/libs.ref/techLEF/xh018_xx51_MET5_METMID.lef.
LEF read: Processed 2312 lines.
Multiple vertical route layers at different pitches.  Using smaller pitch 0.63, will route on 1-of-N tracks if necessary.
Reading LEF data from file /ef/tech/XFAB.3/EFXH018C/libs.ref/lef/D_CELLS/xh018_D_CELLS.lef.
LEF file:  Defines site core (ignored)
LEF read: Processed 84298 lines.
Multiple vertical route layers at different pitches.  Using smaller pitch 0.63, will route on 1-of-N tracks if necessary.
Reading DEF data from file frequency_divider.def.
Diagnostic: Design name: "frequency_divider"
Multiple vertical route layers at different pitches.  Using pitch 0.63 and routing on 1-of-N tracks for larger pitches.
  Processed 264 subcell instances total.
  Processed 11 pins total.
  Processed 244 nets total.
LEF Read, Line 1385: Via "VIA1_X_so" does not define a metal layer!
LEF Read, Line 1386: Via "VIA1_X_so" does not define a metal layer!
LEF Read, Line 1387: Via "VIA1_X_so" does not define a metal layer!
LEF Read, Line 1389: Via "VIA2_so" does not define a metal layer!
LEF Read, Line 1390: Via "VIA2_so" does not define a metal layer!
LEF Read, Line 1391: Via "VIA2_so" does not define a metal layer!
LEF Read, Line 1393: Via "VIA3_so" does not define a metal layer!
LEF Read, Line 1394: Via "VIA3_so" does not define a metal layer!
LEF Read, Line 1395: Via "VIA3_so" does not define a metal layer!
LEF Read, Line 1397: Via "VIA4_so" does not define a metal layer!
LEF Read, Line 1398: Via "VIA4_so" does not define a metal layer!
LEF Read, Line 1399: Via "VIA4_so" does not define a metal layer!
LEF Read, Line 1401: Via "VIATP_X_so" does not define a metal layer!
LEF Read, Line 1402: Via "VIATP_X_so" does not define a metal layer!
LEF Read, Line 1404: Via "VIA1_X_so" does not define a metal layer!
LEF Read, Line 1405: Via "VIA1_X_so" does not define a metal layer!
LEF Read, Line 1406: Via "VIA1_X_so" does not define a metal layer!
```

POST STA

/home/elmioiti/design/P_frequency_divider_bak/qflow/log/post_sta.log

```
Qflow static timing analysis logfile created on Sat Aug 4 04:24:54 PDT 2018
Converting qrouter output to vesta delay format
Running rc2dly -r frequency_divider.rc -l /ef/tech/XFAB.3/EFXH018C/libs.ref/liberty/D_CELLS/D_CELLS_LPMOS_typ_1_80V_25C.lib -d frequency_divider.dly
Converting qrouter output to SPEF delay format
Running rc2dly -r frequency_divider.rc -l /ef/tech/XFAB.3/EFXH018C/libs.ref/liberty/D_CELLS/D_CELLS_LPMOS_typ_1_80V_25C.lib -d frequency_divider.spef
Converting qrouter output to SDF delay format
Running rc2dly -r frequency_divider.rc -l /ef/tech/XFAB.3/EFXH018C/libs.ref/liberty/D_CELLS/D_CELLS_LPMOS_typ_1_80V_25C.lib -d frequency_divider.sdf
Running vesta static timing analysis with back-annotated extracted wire delays
vesta -c -d frequency_divider.dly --long frequency_divider.rtlnopwr.v /ef/tech/XFAB.3/EFXH018C/libs.ref/liberty/D_CELLS/D_CELLS_LPMOS_typ_1_80V_25C.lib
----------------------------------------
Vesta static timing analysis tool
(c) 2013-2017 Tim Edwards, Open Circuit Design
----------------------------------------

Parsing library "D_CELLS_LPMOS_typ_1_80V_25C"
End of library at line 426120
Parsing module "frequency_divider"
Lib Read:  Processed 426121 lines.
Verilog netlist read:  Processed 248 lines.
Number of paths analyzed:  29

Top 20 maximum delay paths:
Path DFFQX4_9/CN to DFFQX4_12/D delay 2169 ps
      1.1 ps              in_bF_buf4:   BUX2_5/Q ->  DFFQX4_9/CN
    605.2 ps  odd_0_initial_begin_1_: DFFQX4_9/Q ->   NO2X1_6/B
    798.9 ps                  _161_:  NO2X1_6/Q ->   NA2X2_1/A
    987.9 ps                  _162_:  NA2X2_1/Q ->  ON31X0_2/C
   1322.2 ps                   _46_: ON31X0_2/Q ->  NA2X0_12/A
   1578.2 ps                   _49_: NA2X0_12/Q ->  AO32X1_3/E
   1988.4 ps                _36__4_: AO32X1_3/Q -> DFFQX4_12/D

Path DFFQX4_11/CN to DFFQX4_13/D delay 1920.29 ps
      2.2 ps              in_bF_buf1:    BUX2_8/Q -> DFFQX4_11/CN
    617.3 ps  odd_0_initial_begin_3_: DFFQX4_11/Q ->   NO3X4_1/B
    864.4 ps                  _149_:   NO3X4_1/Q ->  AND3X4_1/A
   1141.5 ps                  _155_:  AND3X4_1/Q ->   NO2X2_3/A
   1309.9 ps                  _156_:   NO2X2_3/Q ->  AO31X0_1/A
   1833.8 ps                _36__5_:  AO31X0_1/Q -> DFFQX4_13/D

Path DFFQX4_11/CN to DFFQX4_5/D delay 1836.62 ps
      2.2 ps              in_bF_buf1:    BUX2_8/Q -> DFFQX4_11/CN
    617.3 ps  odd_0_initial_begin_3_: DFFQX4_11/Q ->   NO3X4_1/B
    864.4 ps                  _149_:   NO3X4_1/Q ->  AND5X4_1/B
   1353.2 ps                   _83_:  AND5X4_1/Q ->  ON21X0_7/A
   1574.6 ps                   _87_:  ON21X0_7/Q ->  NA22X0_3/B
   1898.3 ps                _34__4_:  NA22X0_3/Q ->  DFFQX4_5/D

Path DFFQX4_2/CN to DFFQX4_6/D delay 1819.72 ps
      0.8 ps          in_bF_buf2:   BUX2_7/Q -> DFFQX4_2/CN
    620.9 ps  odd_0_counter2_1_: DFFQX4_2/Q ->  NO2X1_9/B
    813.6 ps                  _77_:  NO2X1_9/Q -> NA3X0_11/C
   1078.3 ps                  _90_: NA3X0_11/Q -> ON21X0_8/B
   1402.0 ps                  _91_: ON21X0_8/Q -> AO32X1_4/C
   1890.5 ps               _34__5_: AO32X1_4/Q -> DFFQX4_6/D

Path DFFQX4_11/CN to DFFQX4_4/D delay 1803.81 ps
      2.2 ps              in_bF_buf1:    BUX2_8/Q -> DFFQX4_11/CN
    617.3 ps  odd_0_initial_begin_3_: DFFQX4_11/Q ->   NO3X4_1/B
    864.5 ps                  _149_:   NO3X4_1/Q ->   NA3X2_1/A
   1090.8 ps                   _71_:   NA3X2_1/Q ->  ON21X0_6/A
   1368.3 ps                   _79_:  ON21X0_6/Q ->  NA22X0_2/B
   1693.9 ps                   _80_:  NA22X0_2/Q ->  NA2X0_16/A
   1865.4 ps                _34__3_:  NA2X0_16/Q ->  DFFQX4_4/D
```

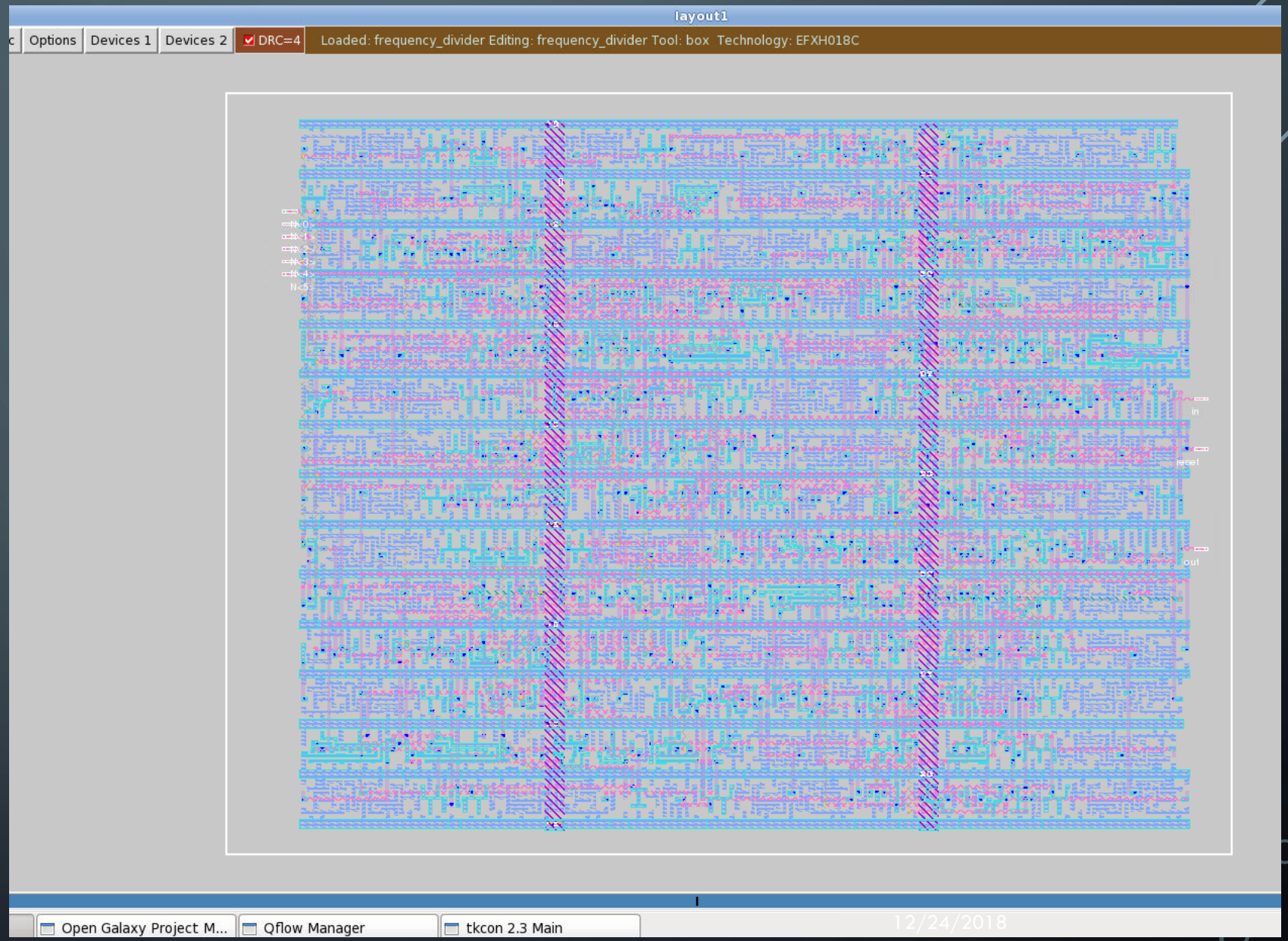
```
   1392.8 ps                   _59_: NA2X0_13/Q -> MU2IX1_2/IN1
   1617.7 ps                   _60_: MU2IX1_2/Q -> MU2IX1_3/IN1
   1817.3 ps                _34__0_: MU2IX1_3/Q -> DFFQX4_1/D

Path DFFQX4_2/CN to DFFQX4_3/D delay 1429.15 ps
      0.8 ps          in_bF_buf2:    BUX2_7/Q ->  DFFQX4_2/CN
    621.4 ps  odd_0_counter2_1_:  DFFQX4_2/Q ->  ON21X0_5/B
    889.5 ps                   _66_:  ON21X0_5/Q -> NO2I1X0_1/AN
   1188.9 ps                   _67_: NO2I1X0_1/Q ->  NA2X0_14/B
   1428.6 ps                   _69_:  NA2X0_14/Q ->  MU2IX1_6/IN1
   1656.4 ps                   _70_:  MU2IX1_6/Q ->  MU2IX1_7/IN1
   1856.5 ps                _34__2_:  MU2IX1_7/Q ->  DFFQX4_3/D

Computed maximum clock frequency (zero slack) = 461.041 MHz
----------------------------------------

Number of paths analyzed:  29

Top 20 minimum delay paths:
Path DFRRQX4_5/C to DFRRQX4_5/D delay 635.953 ps
      0.9 ps          in_bF_buf0:    BUX2_9/Q -> DFRRQX4_5/C
    481.7 ps  even_0_counter_5_: DFRRQX4_5/Q ->  AN31X1_1/D
    545.1 ps                   _31_:  AN31X1_1/Q ->   NO2X0_3/A
    608.3 ps                _2__5_:   NO2X0_3/Q -> DFRRQX4_5/D

Path DFRSQX4_1/C to DFRSQX4_1/D delay 670.547 ps
      1.0 ps          in_bF_buf1:    BUX2_8/Q -> DFRSQX4_1/C
    400.8 ps  even_0_counter_0_: DFRSQX4_1/Q -> NA2I1X0_2/B
    490.4 ps                   _13_: NA2I1X0_2/Q ->   NA3X0_3/B
    611.8 ps                _2__0_:   NA3X0_3/Q -> DFRSQX4_1/D

Path DFRSQX4_2/C to DFRSQX4_2/D delay 710.343 ps
      0.7 ps           in_bF_buf0:    BUX2_9/Q -> DFRSQX4_2/C
    357.2 ps  even_0_out_counter: DFRSQX4_2/Q ->  ON31X0_1/D
    470.9 ps                    _7_:  ON31X0_1/Q ->   NA2X0_2/A
    563.1 ps                    _3_:   NA2X0_2/Q -> DFRSQX4_2/D

Path DFRQX4_4/C to DFRRQX4_6/D delay 722.591 ps
      1.6 ps       in_bF_buf3:    BUX2_6/Q ->  DFRQX4_4/C
    370.2 ps  odd_0_old_N_3_:  DFRQX4_4/Q ->   NO2X2_2/B
    439.5 ps                   _136_:   NO2X2_2/Q -> NO3I1X2_2/B
    505.3 ps                   _139_: NO3I1X2_2/Q ->  AN32X1_1/B
    625.9 ps                    _39_:  AN32X1_1/Q -> DFRRQX4_6/D

Path DFRQX4_9/C to DFRQX4_9/D delay 733.052 ps
      2.0 ps          in_bF_buf3:   BUX2_6/Q -> DFRQX4_9/C
    462.7 ps  odd_0_counter_2_: DFRQX4_9/Q ->  NO2X2_7/B
    560.4 ps                   _107_:  NO2X2_7/Q ->  NO3X2_2/C
    636.2 ps                   _109_:  NO3X2_2/Q -> MU2IX1_8/IN1
    724.0 ps                _35__2_: MU2IX1_8/Q -> DFRQX4_9/D

Path DFFQX4_11/CN to DFFQX4_11/D delay 753.119 ps
      2.2 ps              in_bF_buf1:    BUX2_8/Q -> DFFQX4_11/CN
    400.1 ps  odd_0_initial_begin_3_: DFFQX4_11/Q ->   NO3X2_1/B
    483.3 ps                  _40_:   NO3X2_1/Q ->  ON21X0_3/B
    585.3 ps                  _42_:  ON21X0_3/Q ->  NA2X0_11/B
    665.1 ps                _36__3_:  NA2X0_11/Q -> DFFQX4_11/D

Path DFRRQX4_4/C to DFRRQX4_4/D delay 761.078 ps
      1.9 ps          in_bF_buf1:    BUX2_8/Q -> DFRRQX4_4/C
    436.8 ps  even_0_counter_4_: DFRRQX4_4/Q ->  ON21X0_2/C
    543.4 ps                   _25_:  ON21X0_2/Q ->   NA3X0_7/C
    663.8 ps                _2__4_:   NA3X0_7/Q -> DFRRQX4_4/D
```

Migration

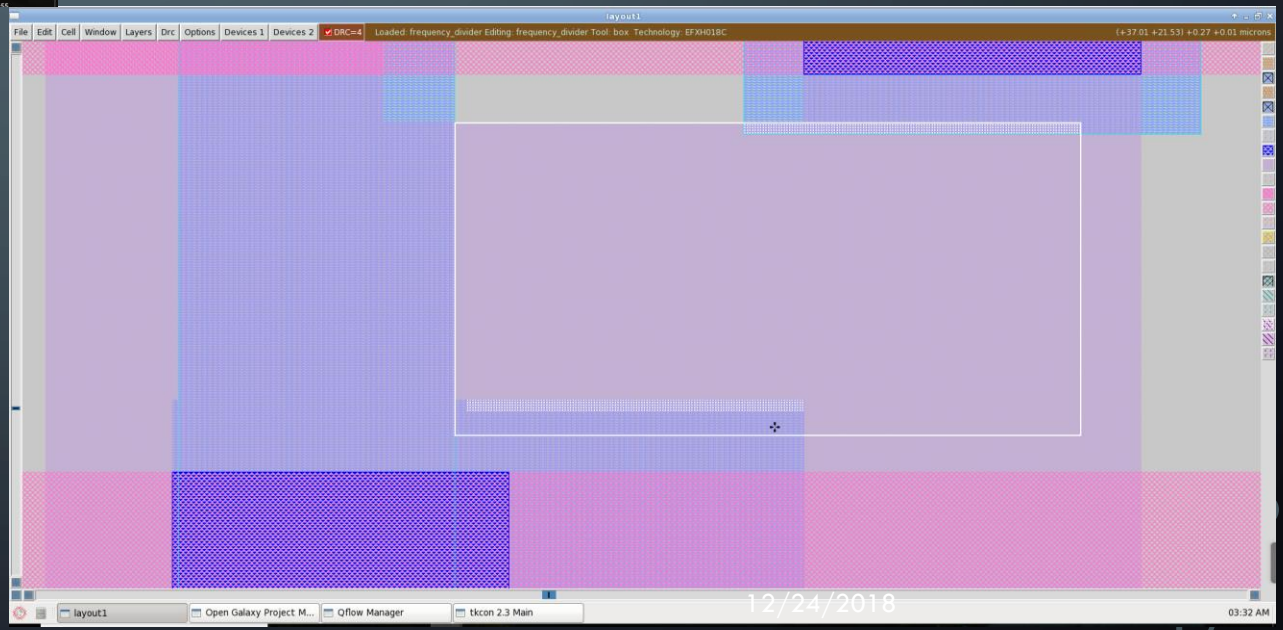
/home/elmioiti/design/P_frequency_divider_bak/mag/comp.out

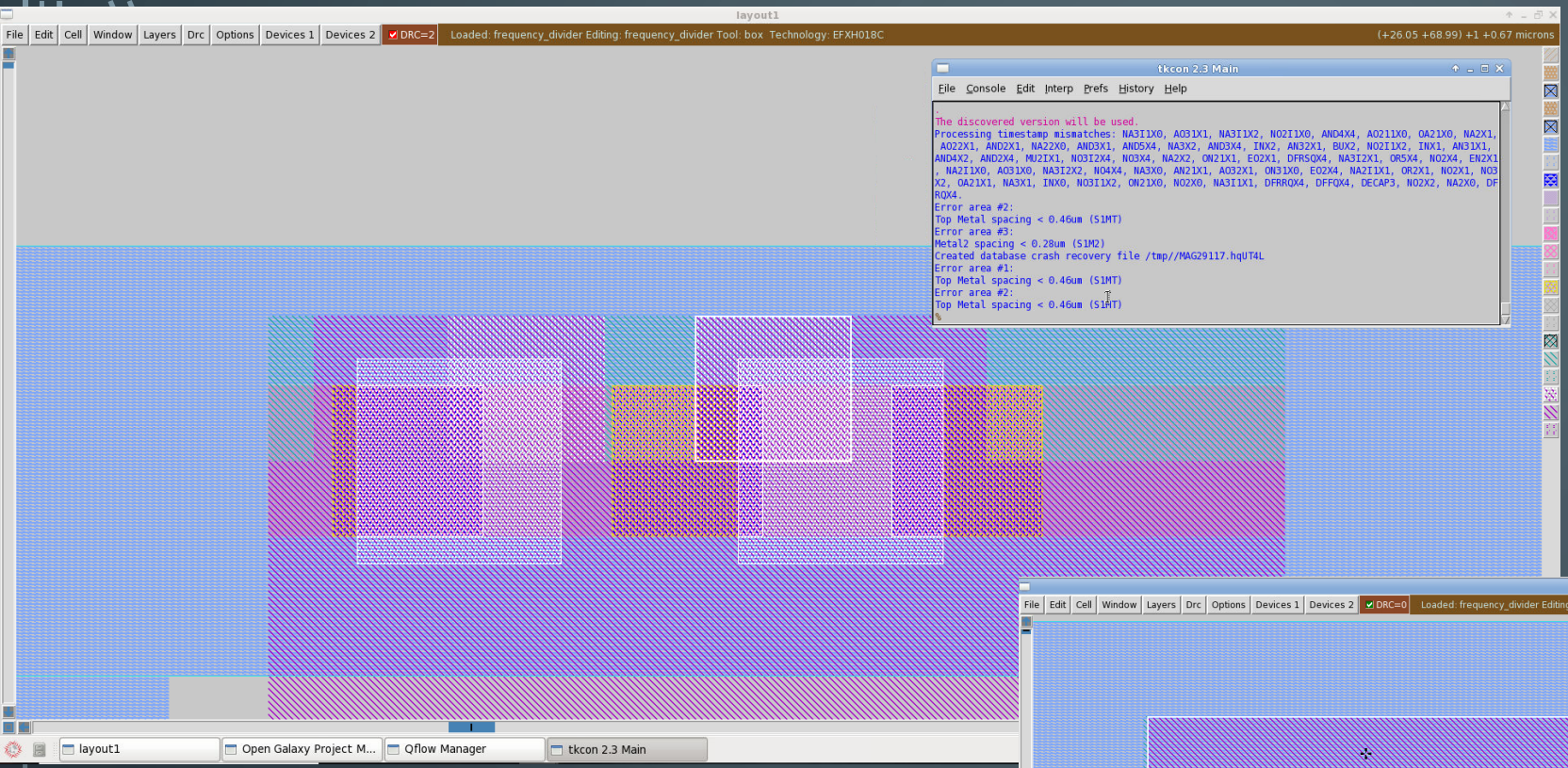
```
EN2X1 (5)                                |EN2X1 (5)
NO2I1X0 (1)                              |NO2I1X0 (1)
AND4X4 (1)                               |AND4X4 (1)
AND3X1 (3)                               |AND3X1 (3)
EO2X1 (3)                                |EO2X1 (3)
NO2I1X2 (2)                              |NO2I1X2 (2)
BUX2 (10)                                |BUX2 (10)
NA3X2 (2)                                |NA3X2 (2)
AN31X1 (2)                               |AN31X1 (2)
AN21X1 (5)                               |AN21X1 (5)
AO22X1 (2)                               |AO22X1 (2)
NA2I1X0 (6)                              |NA2I1X0 (6)
NA22X0 (3)                               |NA22X0 (3)
NA3X1 (6)                                |NA3X1 (6)
AO211X0 (1)                              |AO211X0 (1)
OA21X0 (1)                               |OA21X0 (1)
AO32X1 (4)                               |AO32X1 (4)
INX1 (4)                                 |INX1 (4)
DFRRQX4 (6)                              |DFRRQX4 (6)
AND5X4 (1)                               |AND5X4 (1)
AND3X4 (1)                               |AND3X4 (1)
NO3I1X2 (2)                              |NO3I1X2 (2)
DFRSQX4 (2)                              |DFRSQX4 (2)
INX2 (1)                                 |INX2 (1)
NA2I1X1 (2)                              |NA2I1X1 (2)
NO2X4 (2)                                |NO2X4 (2)
AN32X1 (1)                               |AN32X1 (1)
AND4X2 (1)                               |AND4X2 (1)
AND2X4 (1)                               |AND2X4 (1)
NO3I2X4 (1)                              |NO3I2X4 (1)
NA2X2 (1)                                |NA2X2 (1)
NA3I2X1 (1)                              |NA3I2X1 (1)
ON31X0 (3)                               |ON31X0 (3)
OR5X4 (1)                                |OR5X4 (1)
AO31X0 (1)                               |AO31X0 (1)
NA3I2X2 (1)                              |NA3I2X2 (1)
OR2X1 (1)                                |OR2X1 (1)
OA21X1 (1)                               |OA21X1 (1)
NA3I1X1 (2)                              |NA3I1X1 (2)
Number of devices: 236                   |Number of devices: 236
Number of nets: 246                      |Number of nets: 246
-------------------------------------------------------------------------------
Circuits match uniquely.
Netlists match uniquely.

Subcircuit pins:
Circuit 1: frequency_divider             |Circuit 2: frequency_divider
-----------------------------------------|-------------------------------------
N<4>                                     |N<4>
out                                      |out
N<0>                                     |N<0>
reset                                    |reset
N<1>                                     |N<1>
in                                       |in
N<3>                                     |N<3>
gnd                                      |gnd! **Mismatch**
vdd                                      |vdd! **Mismatch**
N<5>                                     |N<5>
N<2>                                     |N<2>
-------------------------------------------------------------------------------
Cell pin lists are equivalent.
Device classes frequency_divider and frequency_divider are equivalent.
Circuits match uniquely.
```

DRC : 4 errors . Minor fixes required!




layout1
File Edit Cell Window Layers Drc Options Devices 1 Devices 2 DRC=4
Loaded: frequency_divider Editing: frequency_divider Tool: box Technology: EFXH018C
(+37.12 +19.6) +0.37 -1.56 microns
tkcon 2.3 Main
File Console Edit Interp Prefs History Help
Warning: Parent cell lists instance of "AO31X1" at bad file path /home/elmioiti/design/P_frequency
_divider_bak/mag/AO31X1.mag.
The cell exists in the search paths at /ef/tech/XFAB.3/EFXH018C/libs.ref/maglef/D_CELLS/AO31X1.mag.
The discovered version will be used.
Warning: Parent cell lists instance of "NA3I1X0" at bad file path /home/elmioiti/design/P_frequenc
y_divider_bak/mag/NA3I1X0.mag.
The cell exists in the search paths at /ef/tech/XFAB.3/EFXH018C/libs.ref/maglef/D_CELLS/NA3I1X0.mag
The discovered version will be used.
Processing timestamp mismatches: NA3I1X0, AO31X1, NA3I1X2, NO2I1X0, AND4X4, AO21X0, OA21X0, NA2X1,
AO22X1, AND2X1, NA22X0, AND3X1, AND5X4, NA3X2, AND3X4, INX2, AN32X1, BUX2, NO2I1X2, INX1, AN31X1,
AND4X2, AND2X4, MU2IX1, NO3I2X4, NO3X4, NA2X2, ON21X1, EO2X1, DFRSQX4, NA3I2X1, OR5X4, NO2X4, EN2X1
, NA2I1X0, AO31X0, NA3I2X2, NO4X4, NA3X0, AN21X1, AO32X1, ON31X0, EO2X4, NA2I1X1, OR2X1, NO2X1, NO3
X2, OA21X1, NA3X1, INX0, NO3I1X2, ON21X0, NO2X0, NA3I1X1, DFRRQX4, DFFQX4, DECAP3, NO2X2, NA2X0, DF
RQX4.
Error area #2:
Top Metal spacing < 0.46um (S1MT)
Error area #3:
layout1
Open Galaxy Project M...
Qflow Manager
tkcon 2.3 Main
03:25 AM


layout1
File Edit Cell Window Layers Drc Options Devices 1 Devices 2 DRC=4
Loaded: frequency_divider Editing: frequency_divider Tool: box Technology: EFXH018C
(+37.01 +21.53) +0.27 +0.01 microns
layout1
Open Galaxy Project M...
Qflow Manager
tkcon 2.3 Main
03:32 AM



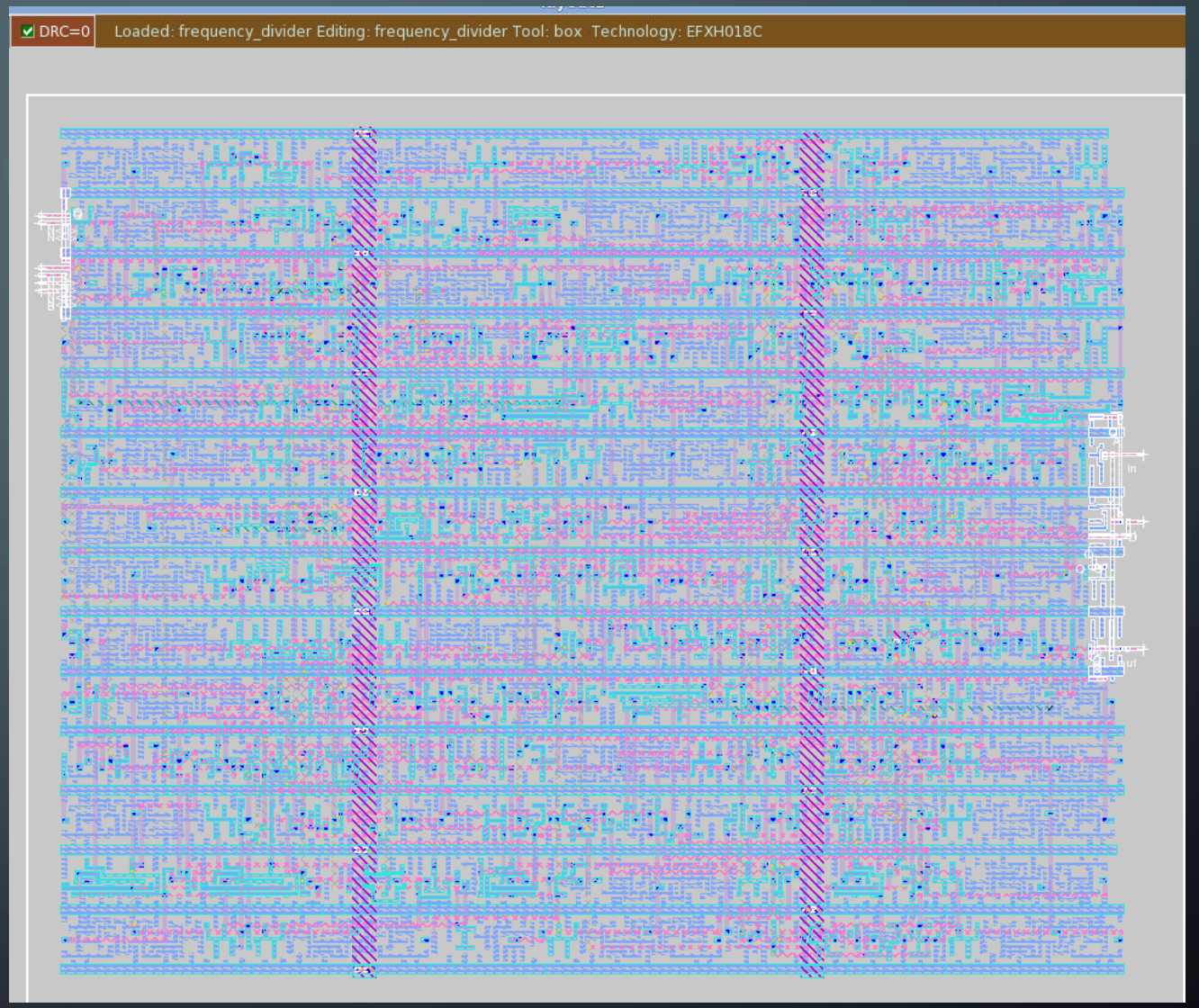
DRC with 2

Finally no DRC in core cell.

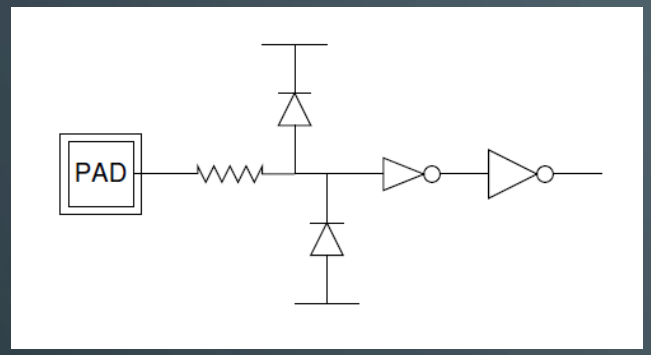
WWW.VLSISYSTEMDESIGN.COM

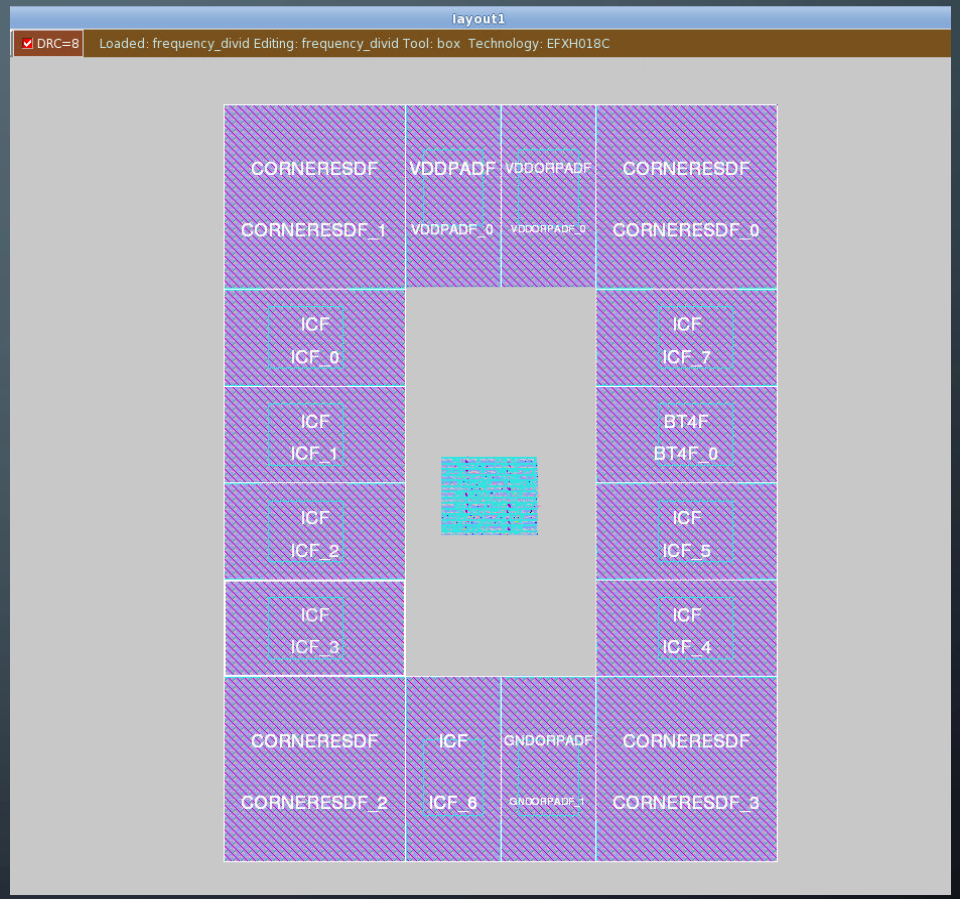
12/24/2018

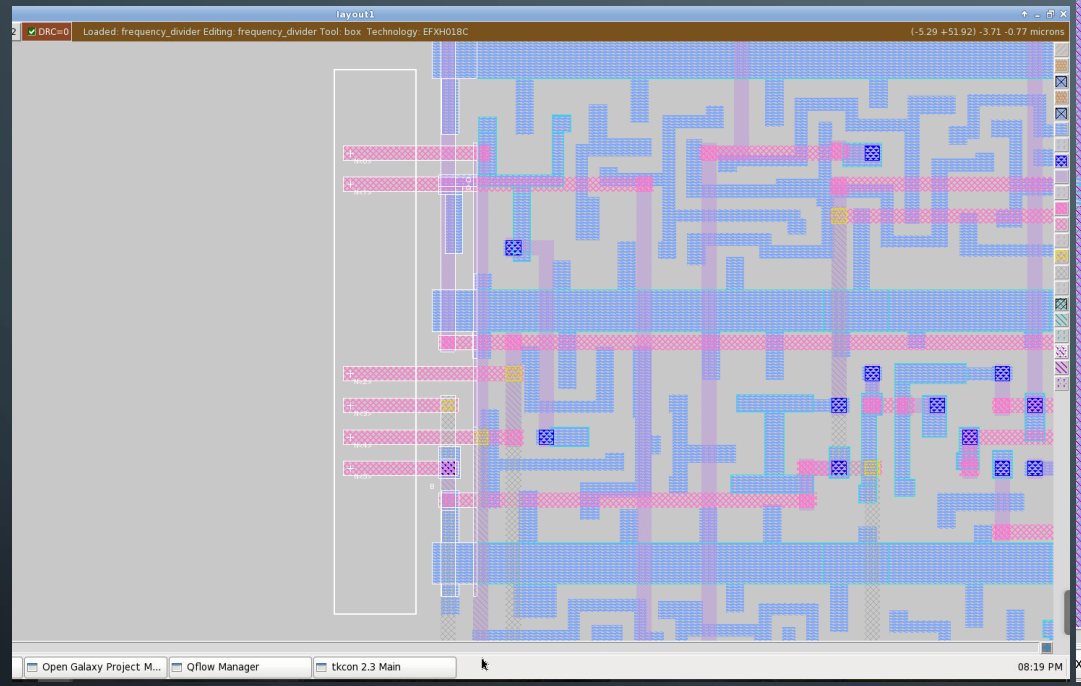
CORE CELL WITH NO DRC

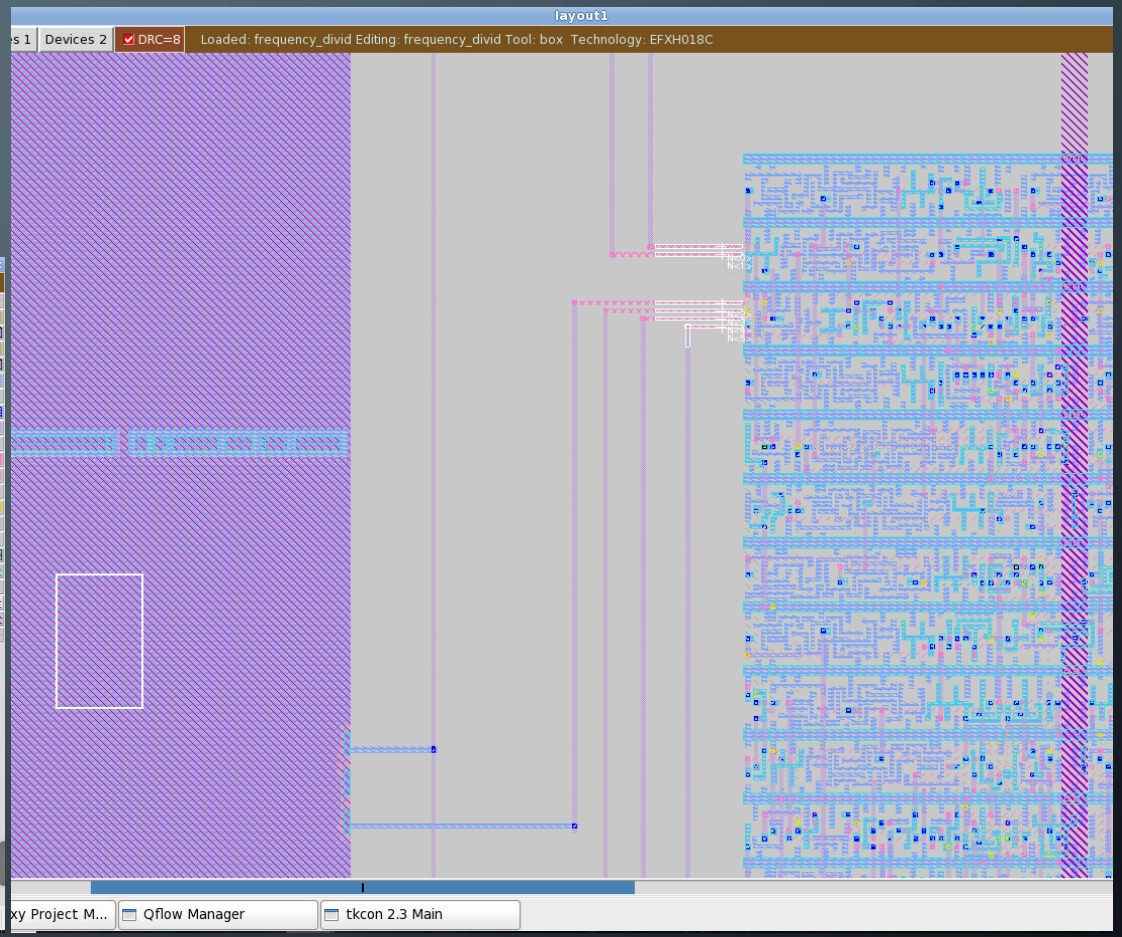


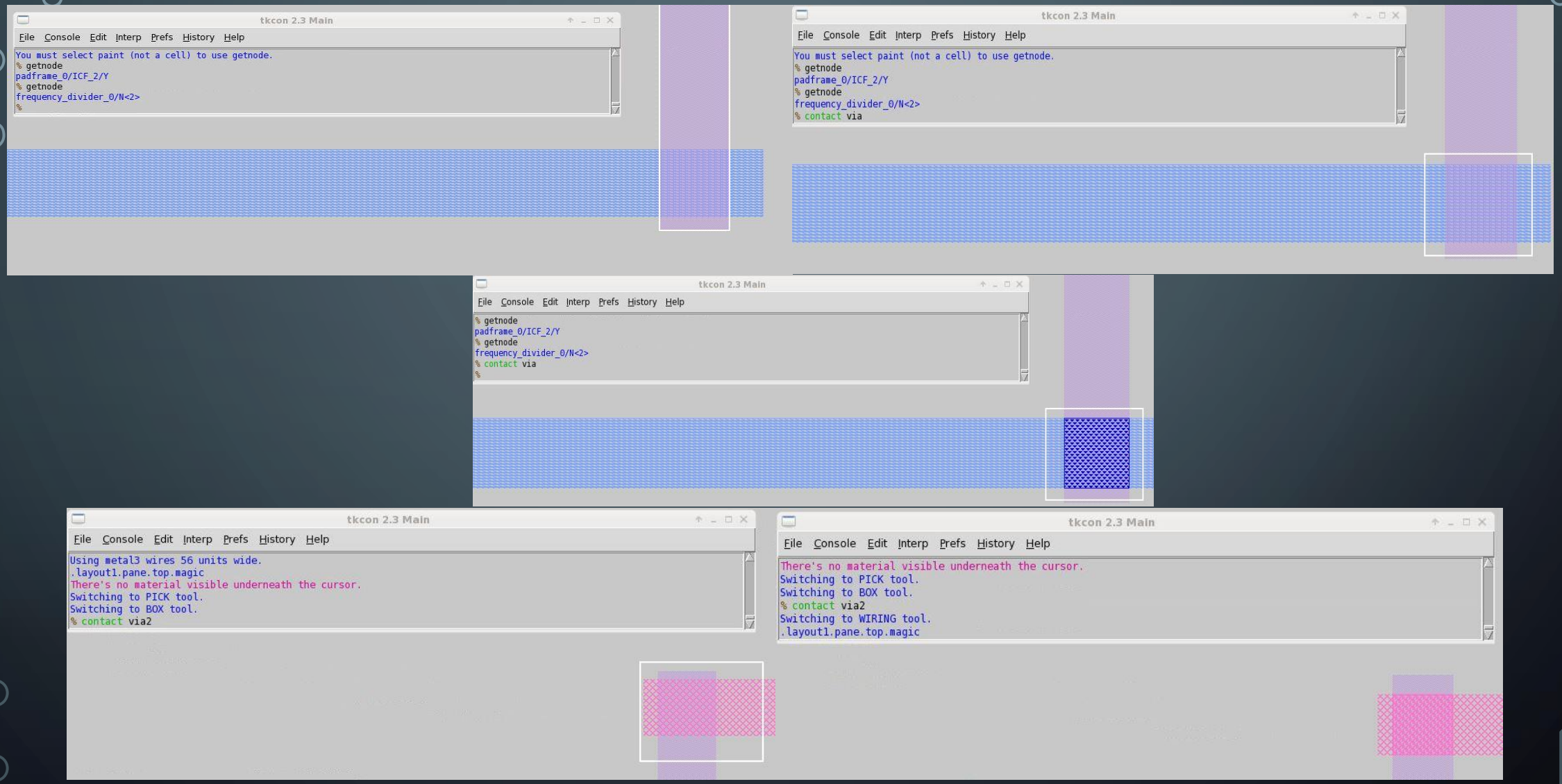
I/O PADS & INTERCONNECTIONS



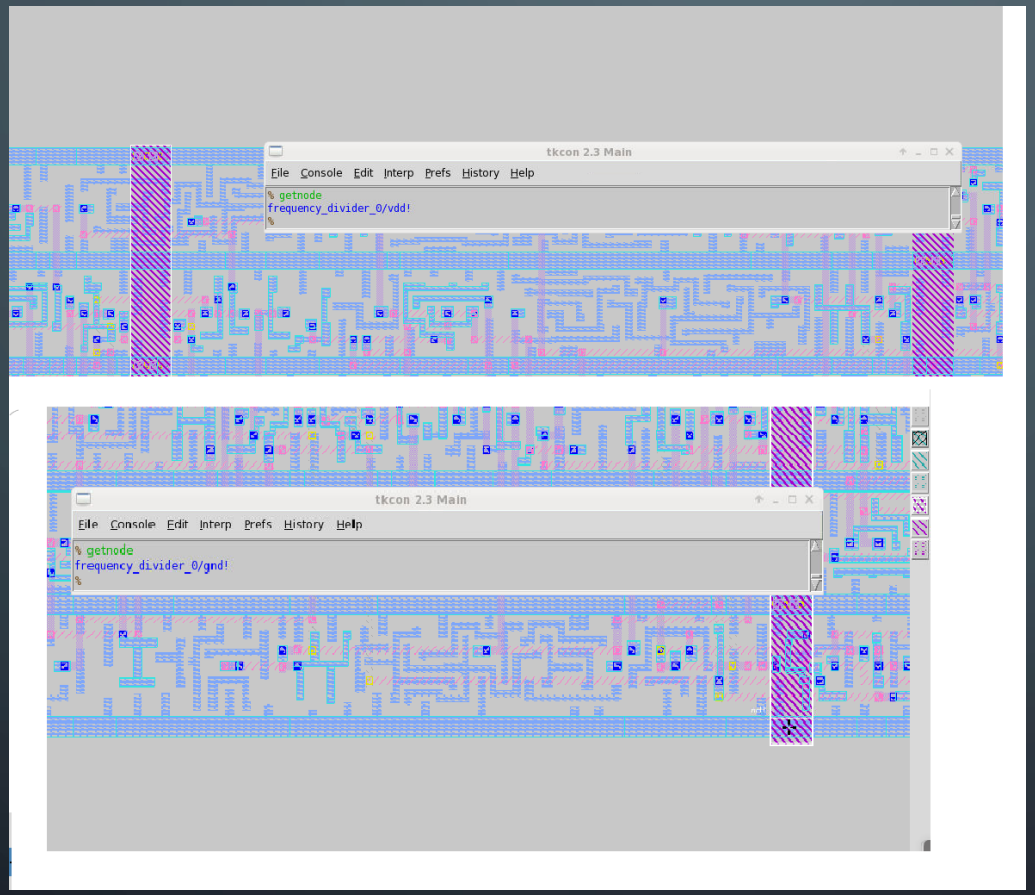


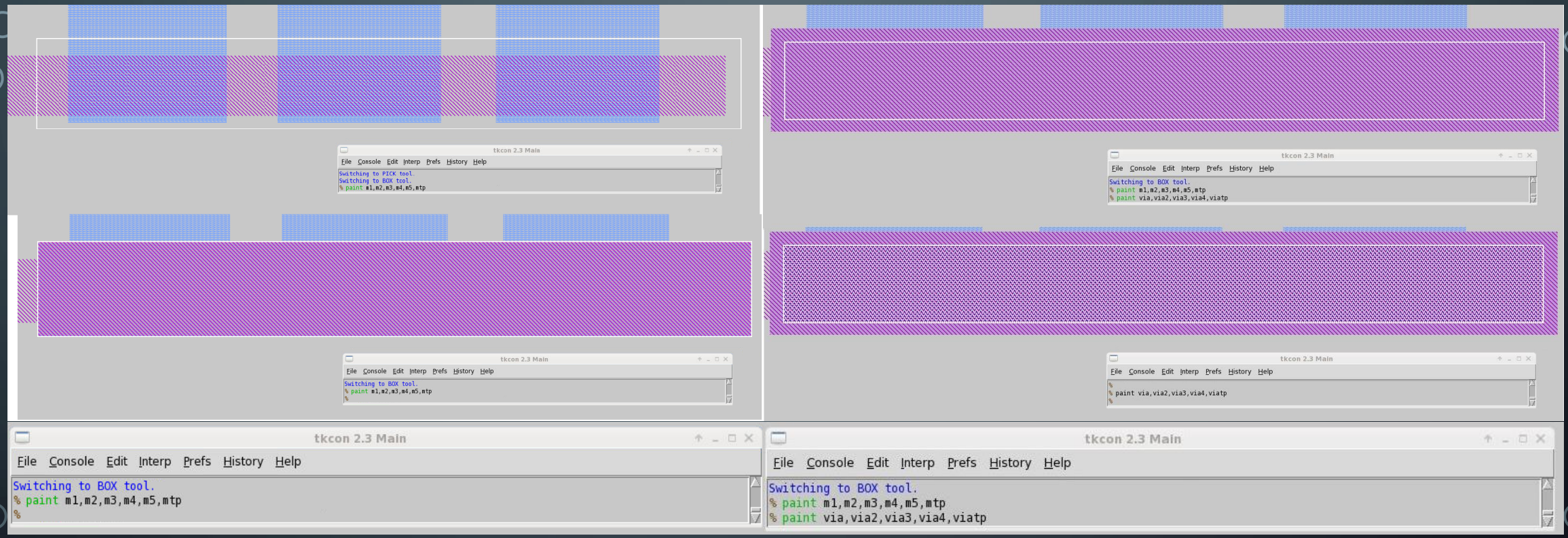

layout1
DRC=0
Loaded: frequency_divider Editing: frequency_divider Tool: box Technology: EFXH018C
(-5.29 +51.92) -3.71 -0.77 microns
Open Galaxy Project M...
Qflow Manager
tkcon 2.3 Main
08:19 PM

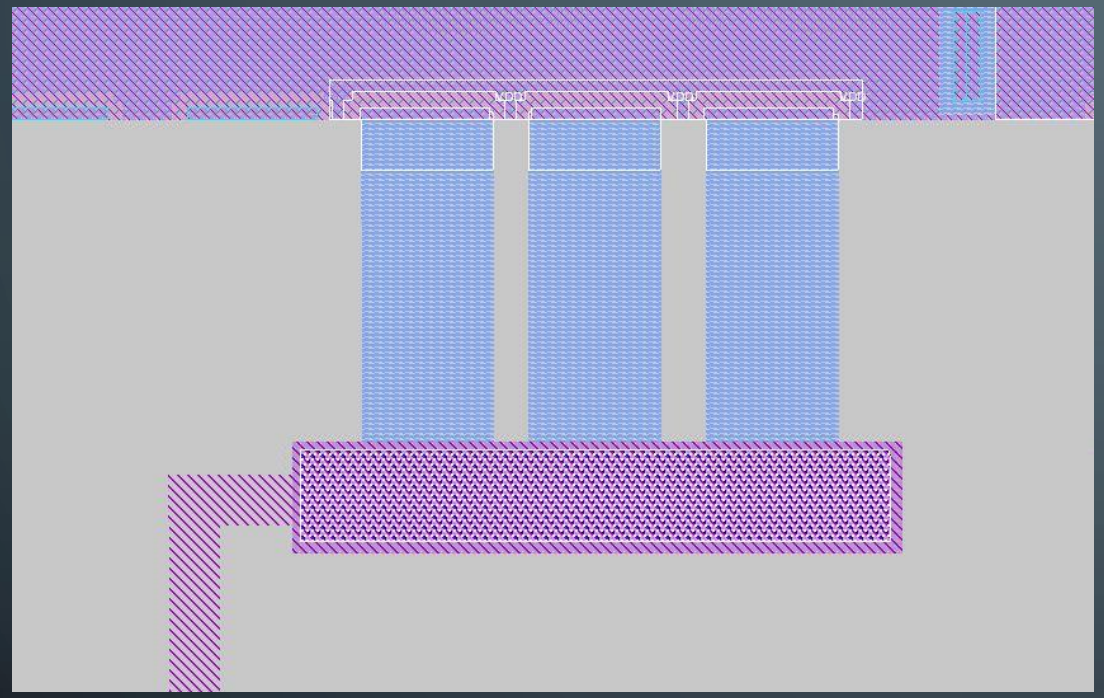

layout1
Devices 2
DRC=8
Loaded: frequency_divid Editing: frequency_divid Tool: box Technology: EFXH018C
Qflow Manager
tkcon 2.3 Main

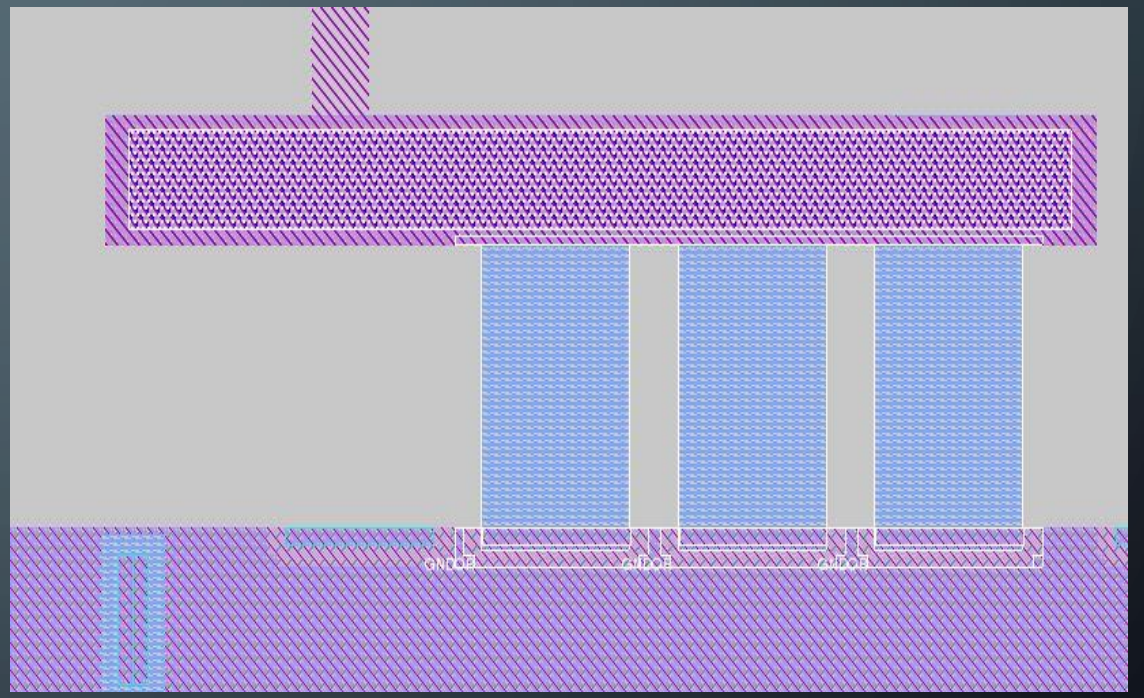

tkcon 2.3 Main
File Console Edit Interp Prefs History Help
You must select paint (not a cell) to use getnode.
% getnode
padframe_0/ICF_2/Y
% getnode
frequency_divider_0/N<2>
%
tkcon 2.3 Main
File Console Edit Interp Prefs History Help
You must select paint (not a cell) to use getnode.
% getnode
padframe_0/ICF_2/Y
% getnode
frequency_divider_0/N<2>
% contact via
tkcon 2.3 Main
File Console Edit Interp Prefs History Help
% getnode
padframe_0/ICF_2/Y
% getnode
frequency_divider_0/N<2>
% contact via
%
tkcon 2.3 Main
File Console Edit Interp Prefs History Help
Using metal3 wires 56 units wide.
.layout1.pane.top.magic
There's no material visible underneath the cursor.
Switching to PICK tool.
Switching to BOX tool.
% contact via2
tkcon 2.3 Main
File Console Edit Interp Prefs History Help
There's no material visible underneath the cursor.
Switching to PICK tool.
Switching to BOX tool.
% contact via2
Switching to WIRING tool.
.layout1.pane.top.magic

POWER & GROUND CONNECTIONS

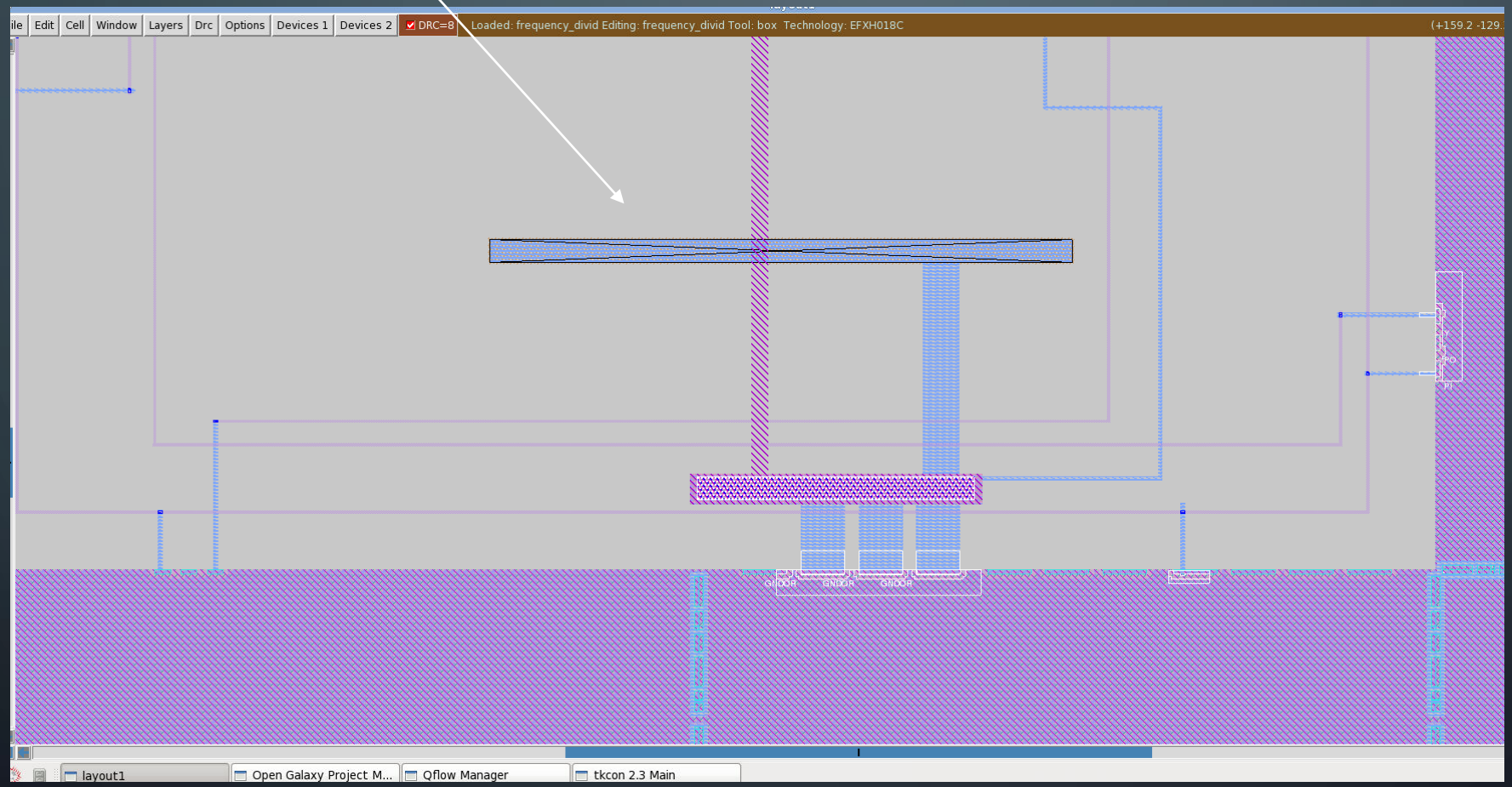



tkcon 2.3 Main
File Console Edit Interp Prefs History Help
Switching to BOX tool.
% paint m1,m2,m3,m4,m5,mtp
%
tkcon 2.3 Main
File Console Edit Interp Prefs History Help
Switching to BOX tool.
% paint m1,m2,m3,m4,m5,mtp
% paint via,via2,via3,via4,viatp

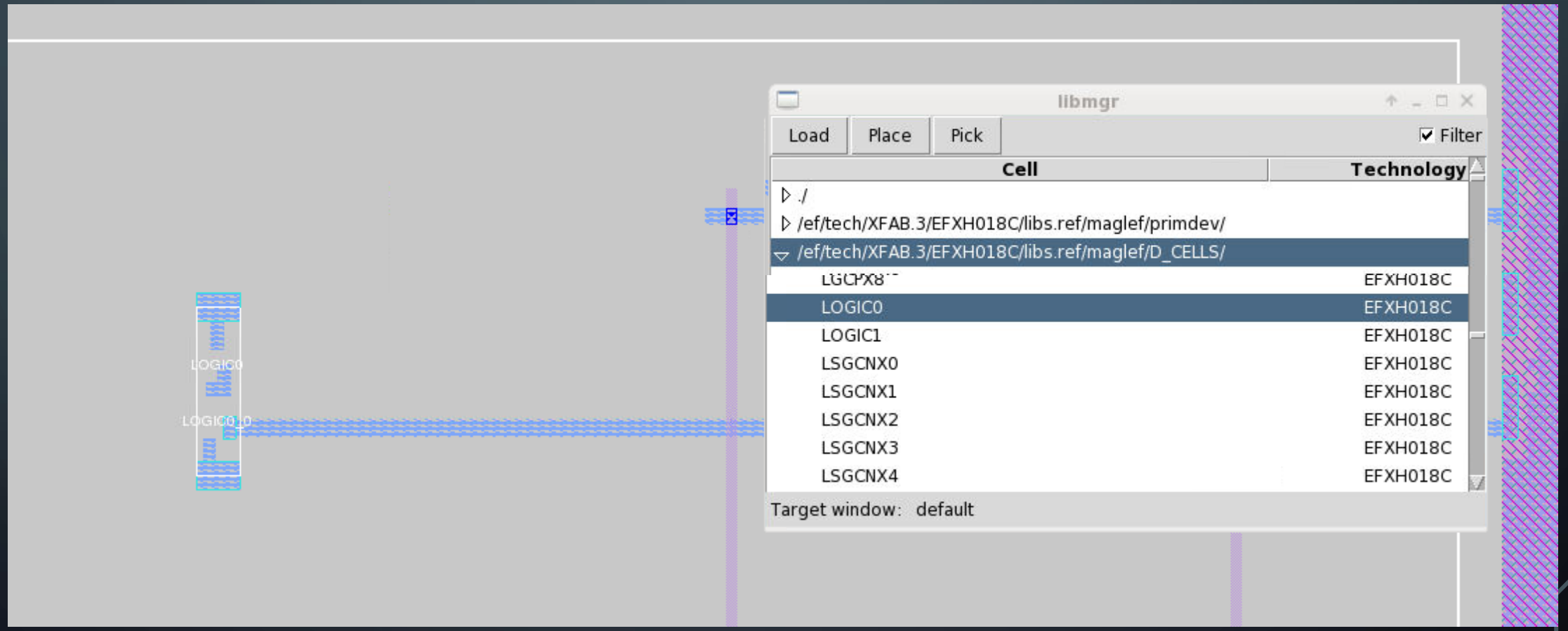




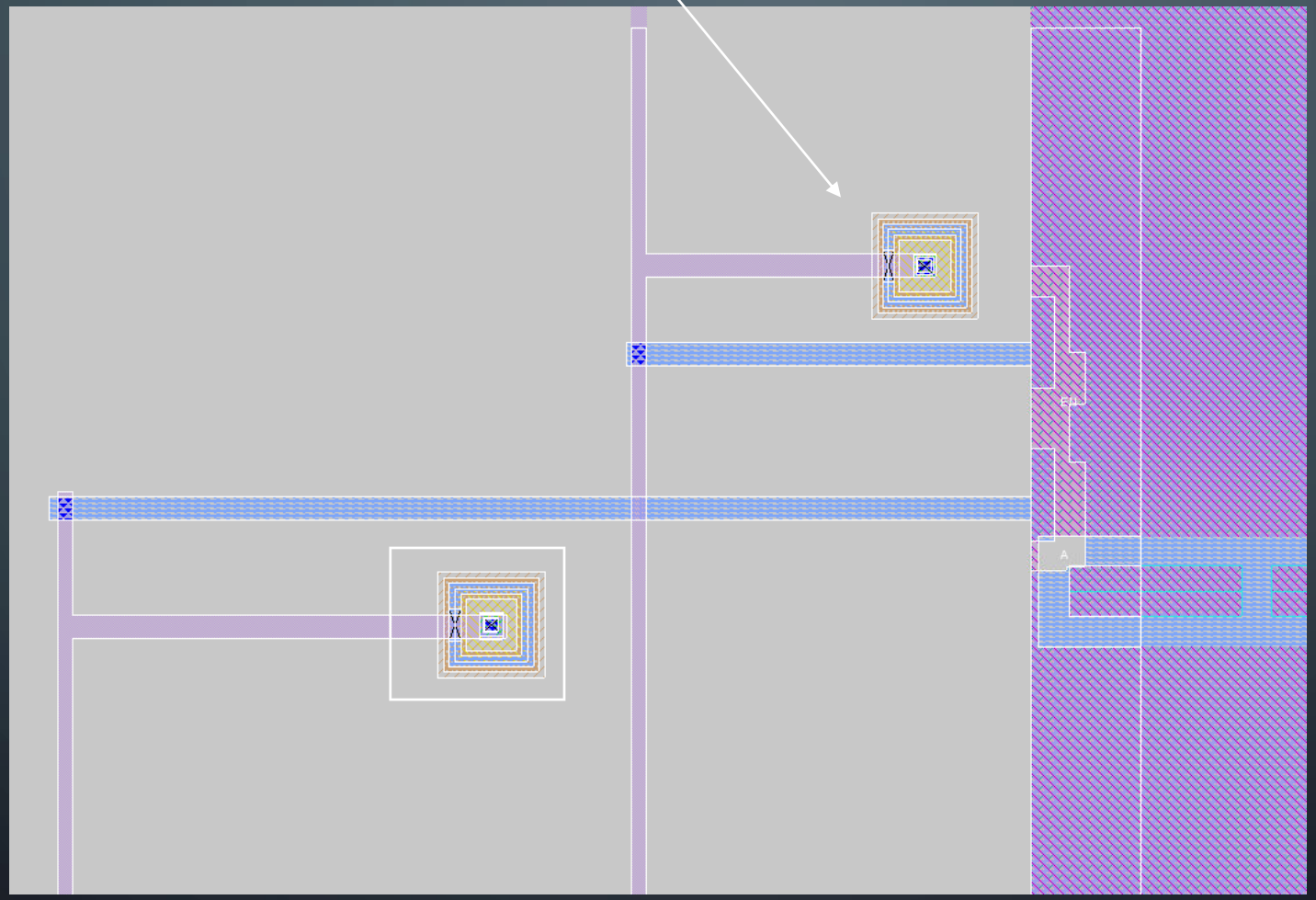
SUBSTRATE CONNECTIONS TO GND PAD



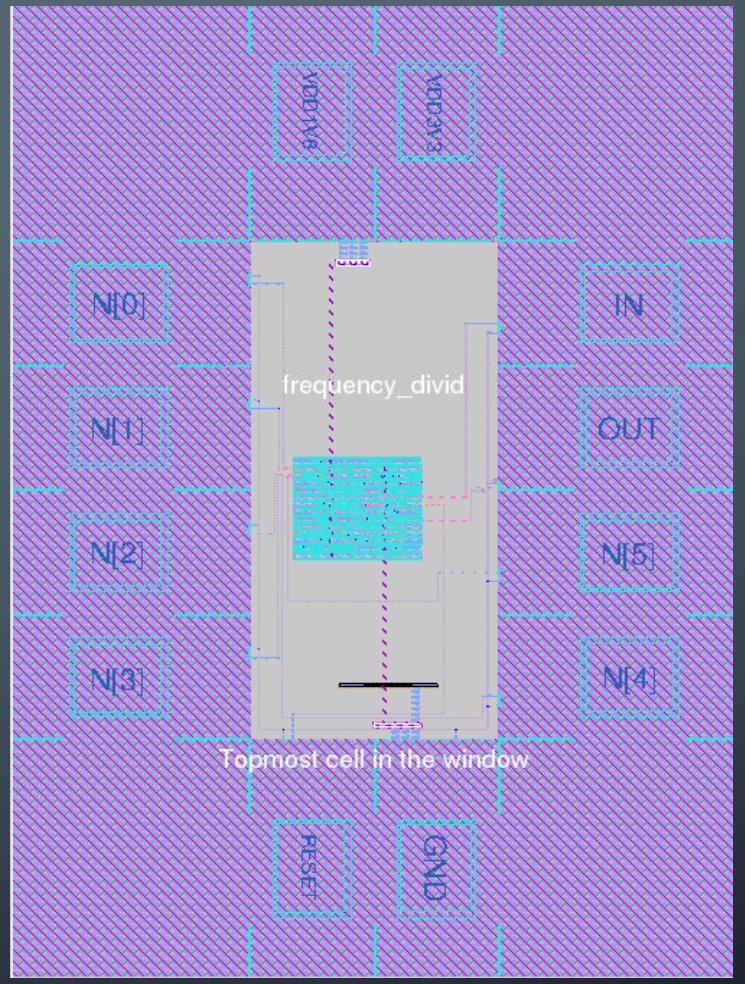
PI CONNECTIONS TO GROUND FOR LVS



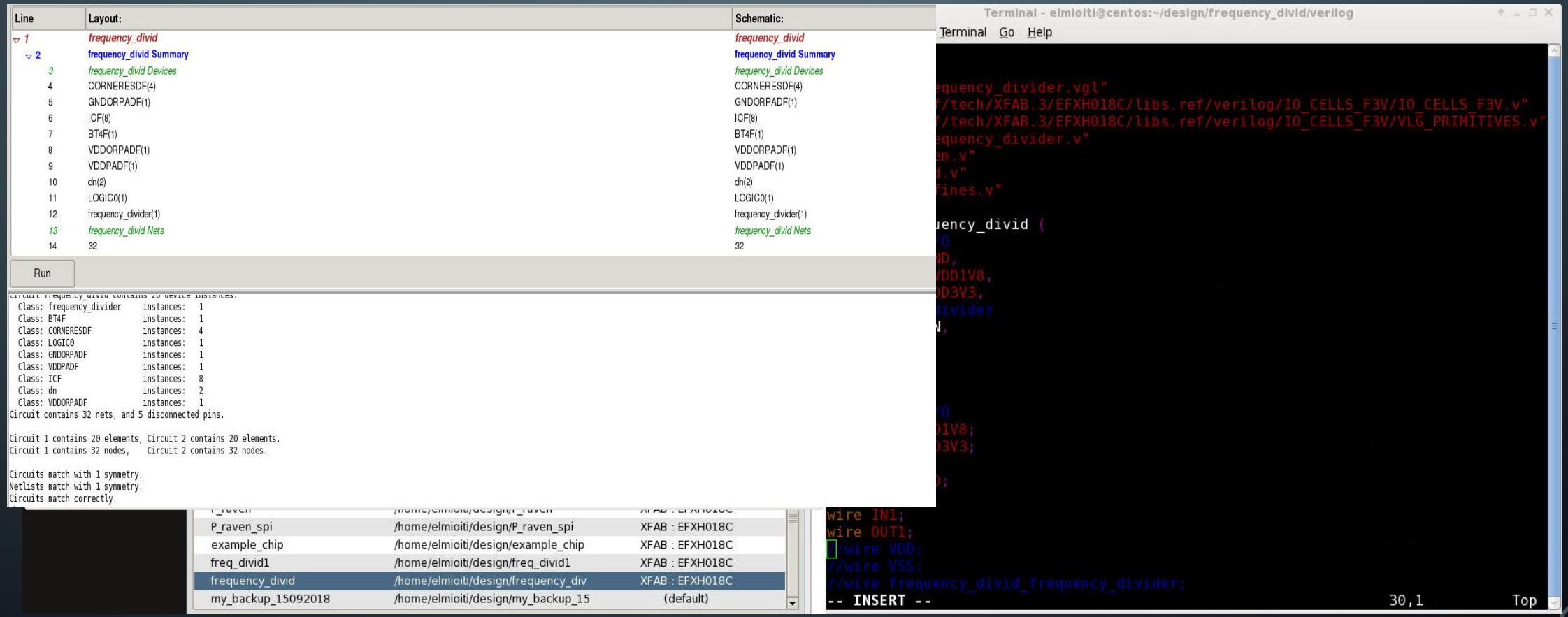
ANTENNA DIODE



FINAL LAYOUT



LVS : LAYOUT VS VERILOG NETLIST IN RUN LVS TOOL



RAPID PHYSICAL IC IMPLEMENTATION AND INTEGRATION USING EFABLESS PLATFORM

ALBERTO GOMEZ SAIZ (AGS@DISROOT.ORG)

MSC. IMPERIAL COLLEGE LONDON

ABSTRACT

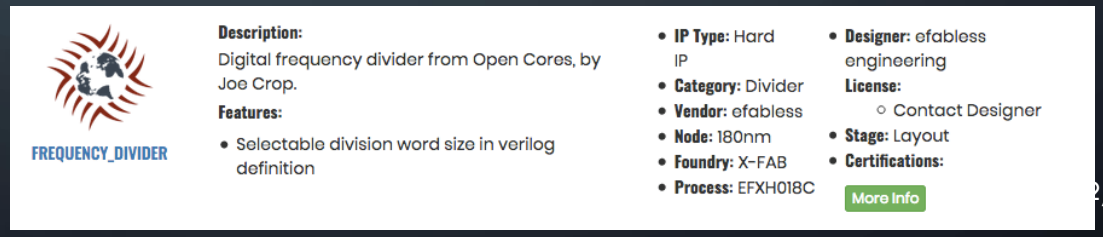
- Bio
- Project description
- Backend flow
  - Physical implementation
  - Top level integration
- Q&A

BIO

- MSc. IC Design, Imperial College London
- Analog IC Designer (>5y)
  - IoT & connectivity
  - Low power data converters
  - Mixed signal design: PLL, ADC
  - Top level chip integration
  - Coder and open-source community member

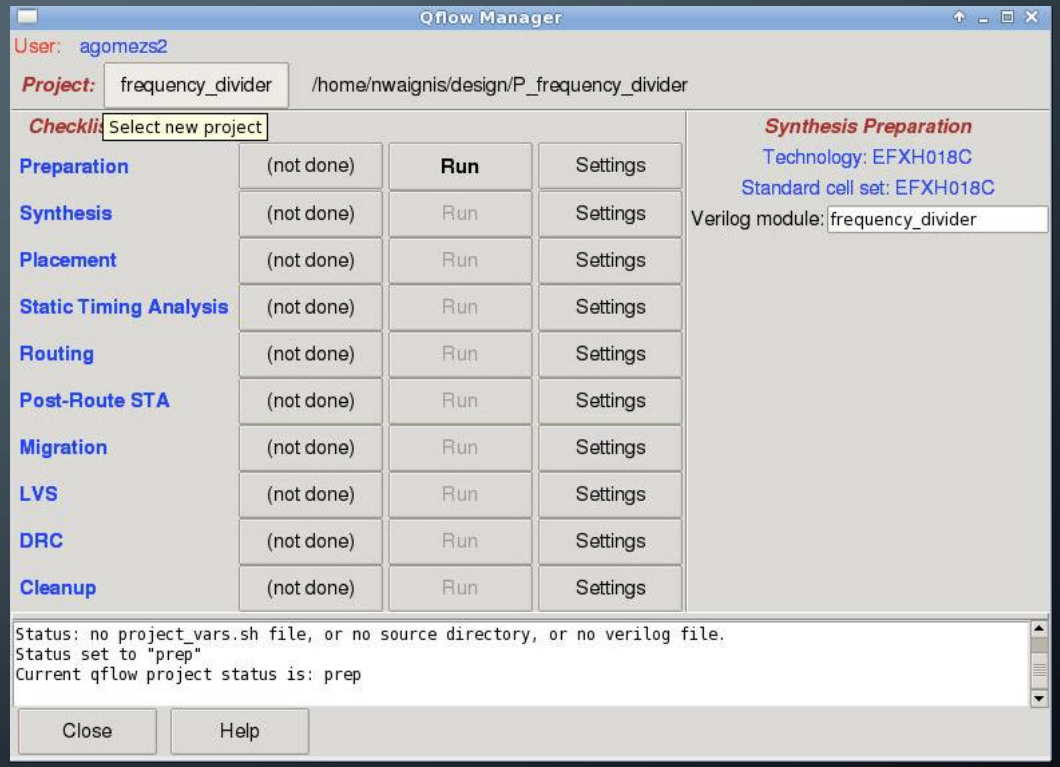
PROJECT DESCRIPTION

- Digital Backend flow for a small RTL design
- Efabless platform
  - Free to access
  - Cloud based
  - Uses open-source tools
- IP:
  - Frequency Divider RTL from Efabless catalog
  - 0.18um XFAB 6M



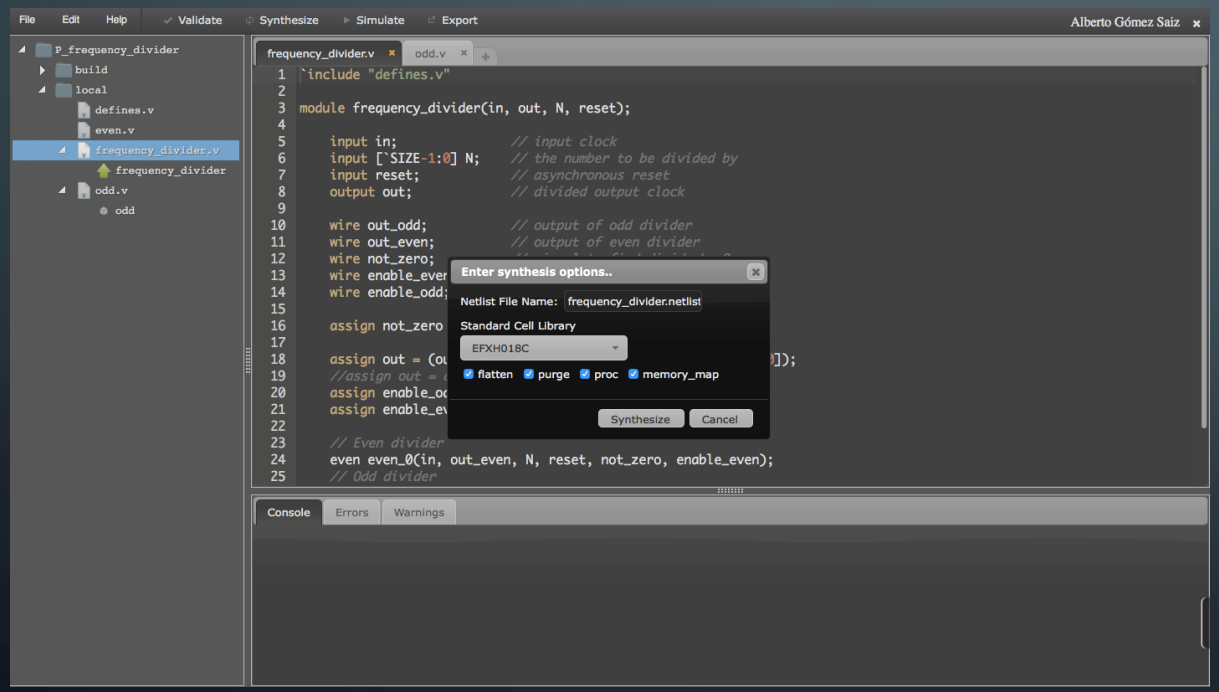
BACKEND FLOW OVERVIEW

- From RTL to Tapeout:
  - Synthesis (CloudV)
  - Placement (qflow GUI)
  - STA & Routing (qflow GUI)
  - LVS & DRC (qflow GUI)
  - Top level integration (Magic VLSI)
  - Top level verification (LVS Manager)



PHYSICAL IMPLEMENTATION: SYNTHESIS

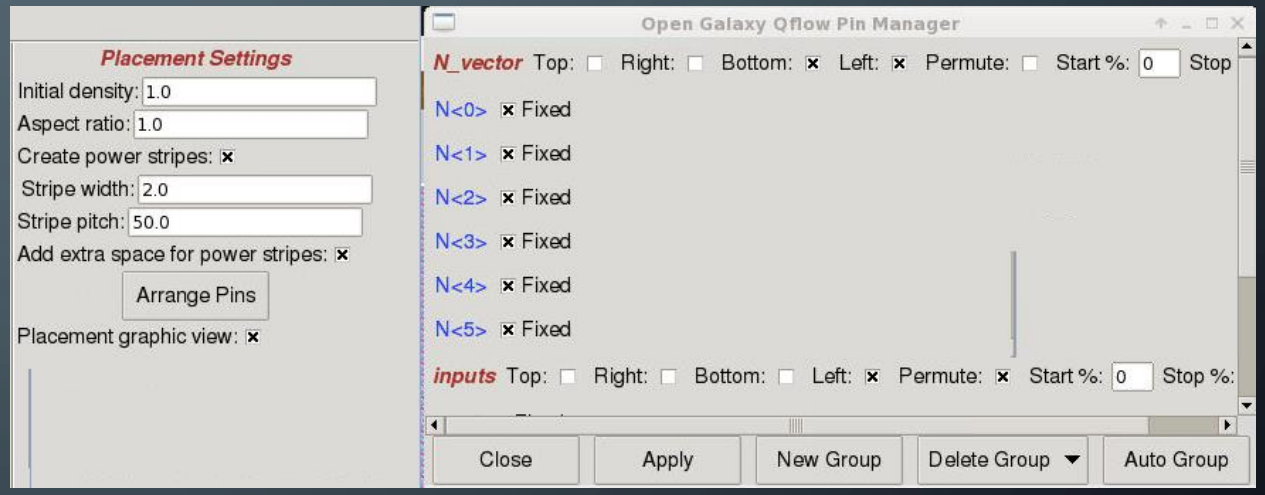
- CloudV: Digital simulator + Synthesis tool




```
11. Printing statistics.

=== frequency_divider ===

   Number of wires:                184
   Number of wire bits:            234
   Number of public wires:         184
   Number of public wire bits:     234
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
   Number of cells:                226
     AN21X0                          5
     AN31X0                          2
     AN32X0                          1
     AND2X0                          3
     AND3X0                          4
     AND4X0                          2
     AND5X0                          1
     AO211X0                         1
     AO22X0                          2
     AO31X0                          2
     AO32X0                          4
     DFFQX0                         13
     DFRQX0                         13
     DFRRQX0                         6
     DFRSQX0                         2
     EN2X0                           5
     EO2X0                           5
     INX0                           21
     MJ2IX0                          8
```

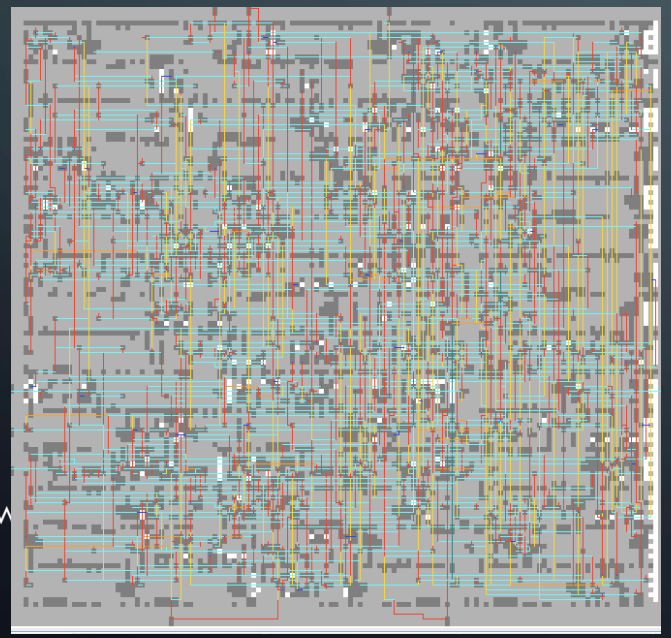
PHYSICAL IMPLEMENTATION: PLACEMENT

- Define block aspect ratio
- Specify Power Stripes
  - Requires power estimation
- Create placement and arrangement pin constrains (GUI)



PHYSICAL IMPLEMENTATION: STA & ROUTING

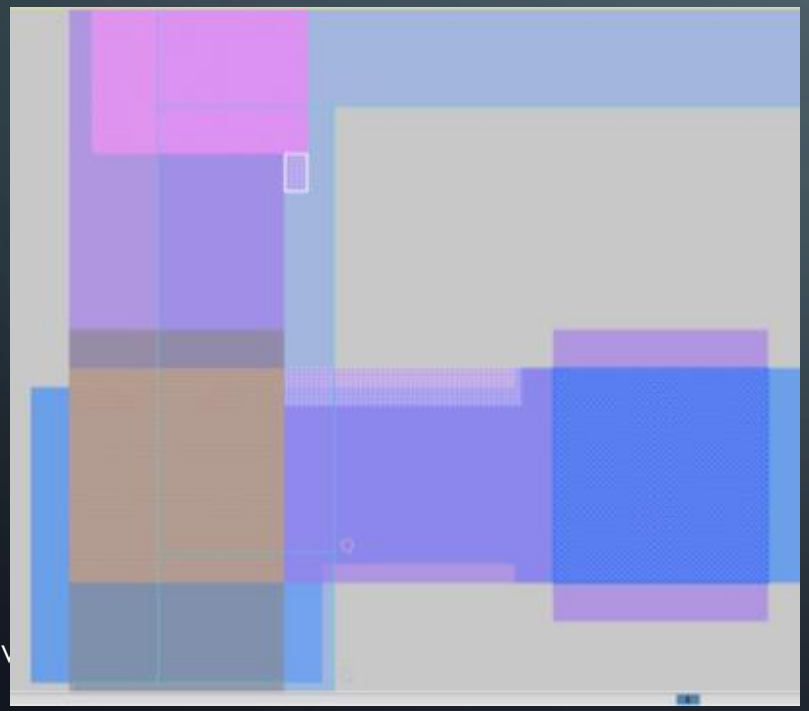
- STA -> max. freq of the design and worst delay path
- Specify number of metal layers for routing
- Post-Route STA recalculates max freq. with routing parasitics

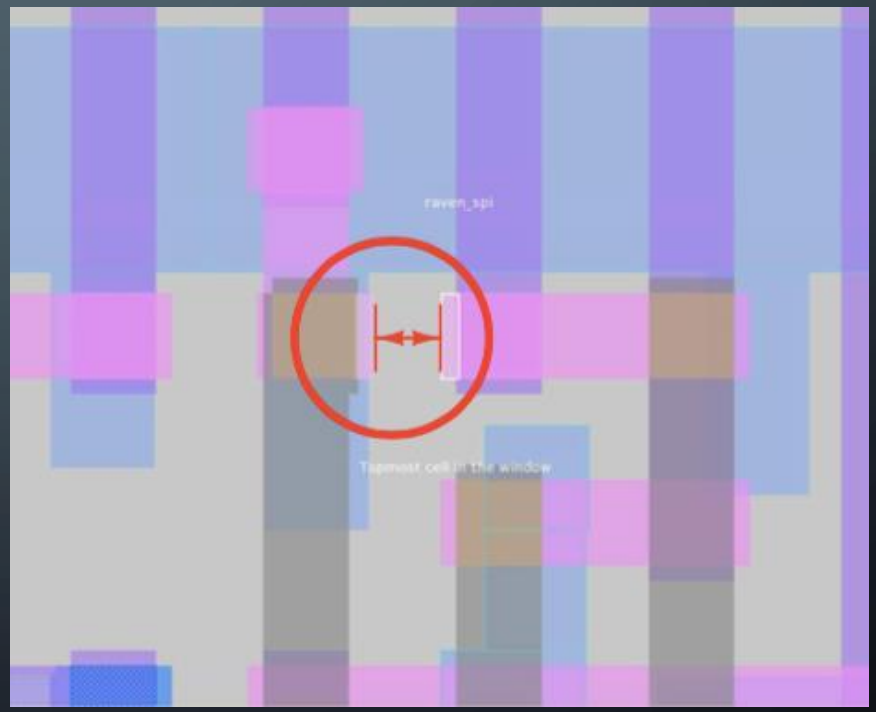


```
Path DFRRQX4_2/C to DFRSQX4_2/D delay 1310.91 ps
      0.0 ps          in_bF_buf1:    BUX2_8/Q -> DFRRQX4_2/C
    457.1 ps  even_0_counter_2_: DFRRQX4_2/Q ->   OR2X1_1/B
    765.9 ps                _4_:   OR2X1_1/Q ->  ON31X0_1/B
   1124.2 ps                _7_:  ON31X0_1/Q ->   NA2X0_2/A
   1362.1 ps                _3_:   NA2X0_2/Q -> DFRSQX4_2/D

Computed maximum clock frequency (zero slack) = 471.809 MHz
----------------------------------------
```

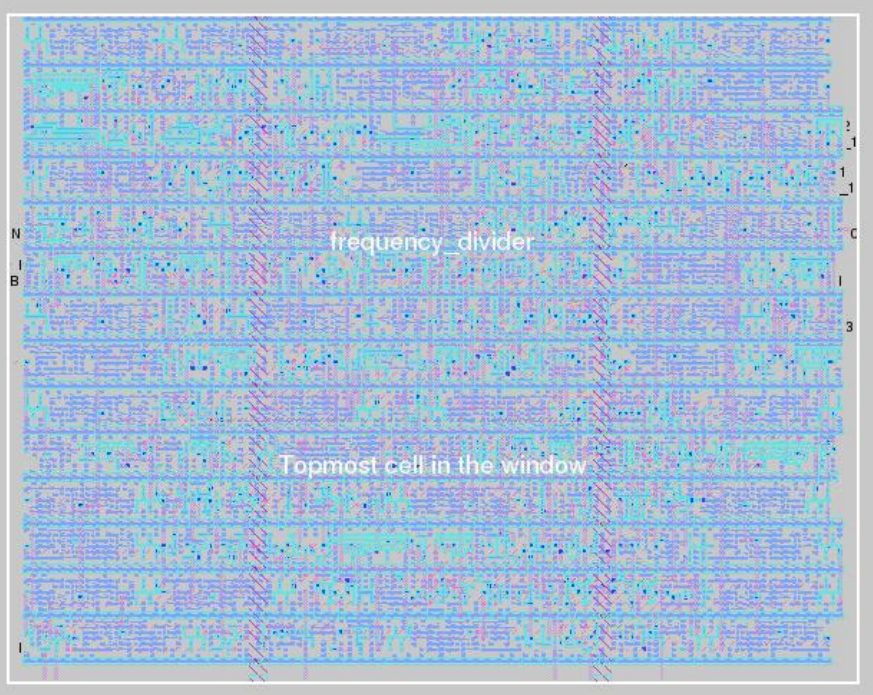
PHYSICAL IMPLEMENTATION: DRC & LVS

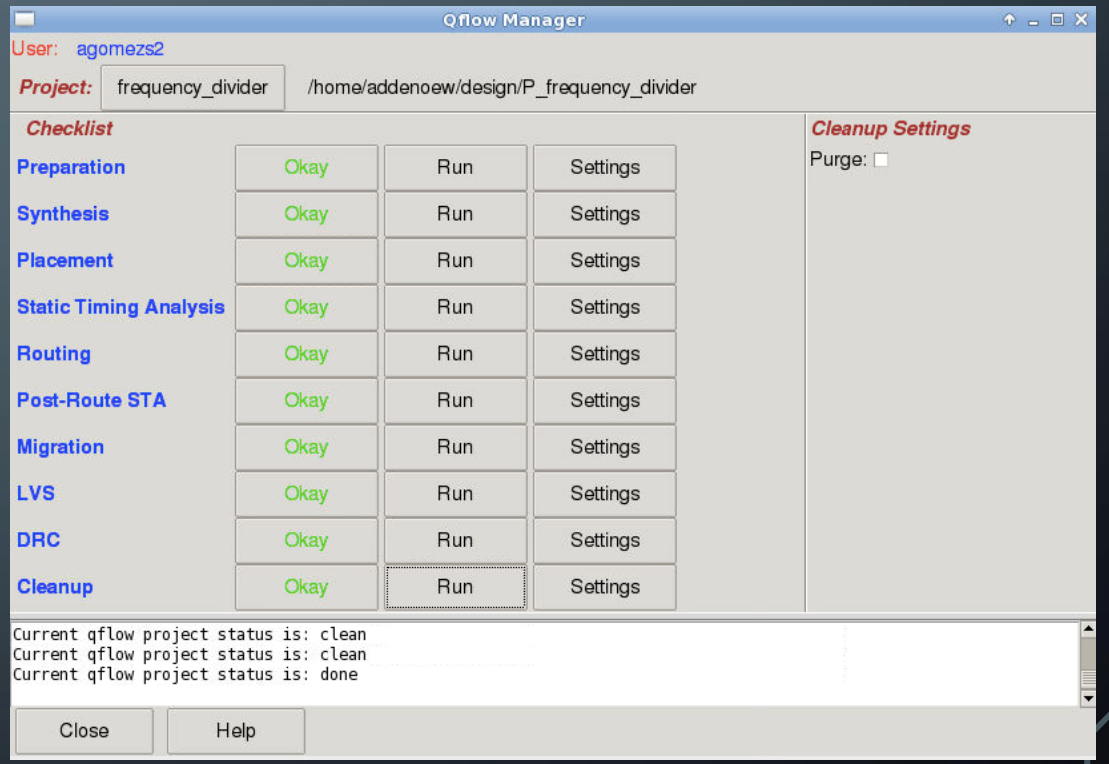
- Using Magic VLSI fix LVS and DRC errors (if any)





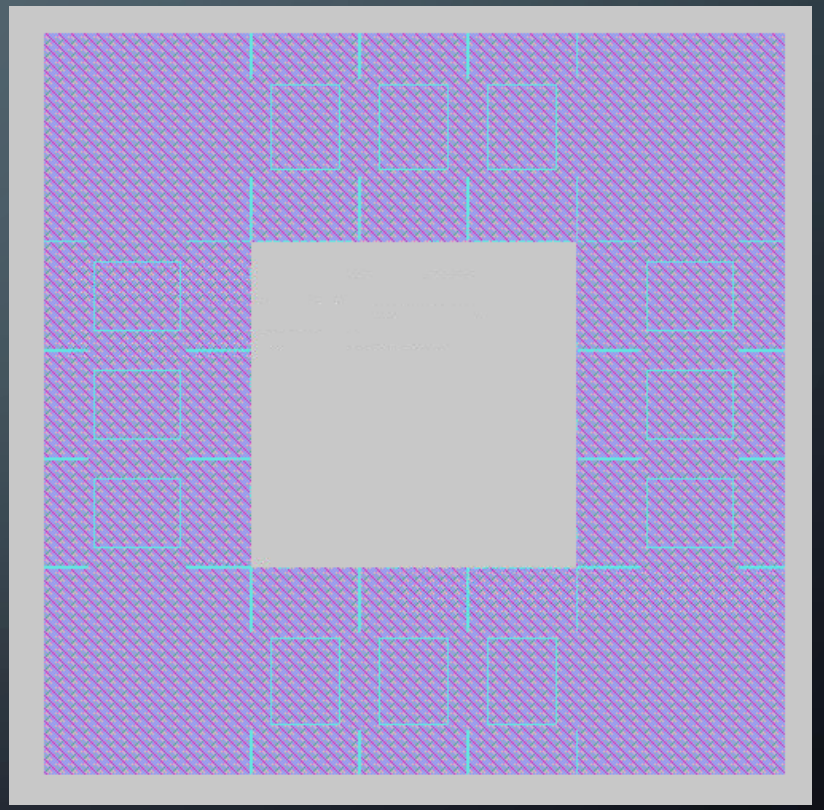
PHYSICAL IMPLEMENTATION: COMPLETED





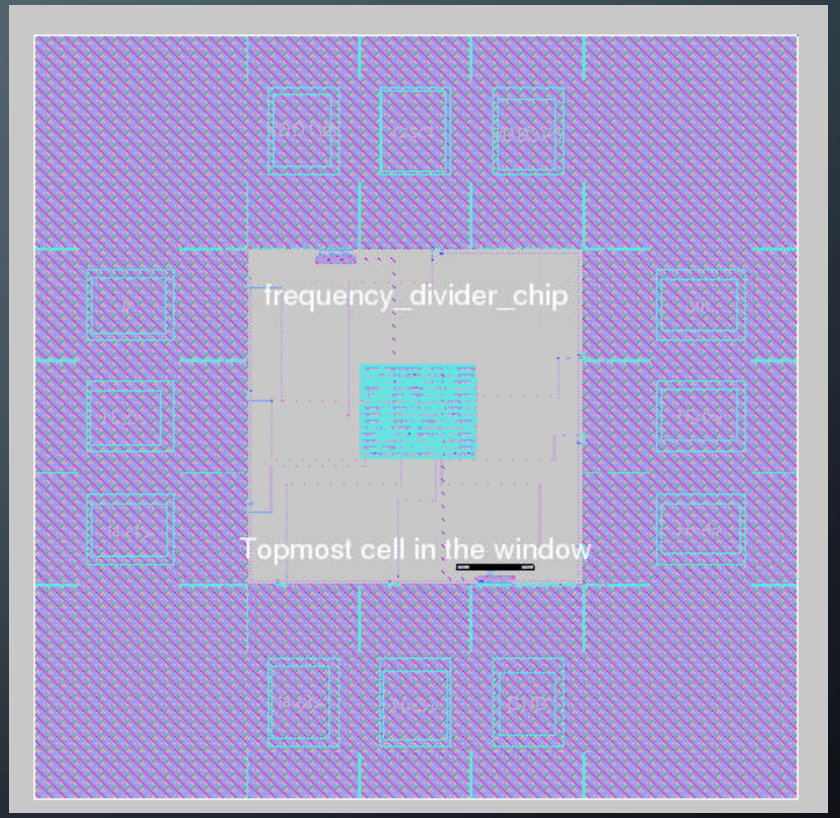
TOP LVL INTEGRATION: PAD RING

- Generate the pad ring
  - Select pads based on IN/OUT requirements
  - Use foundry cells (ESD protected)
  - If design core limited uses fillers



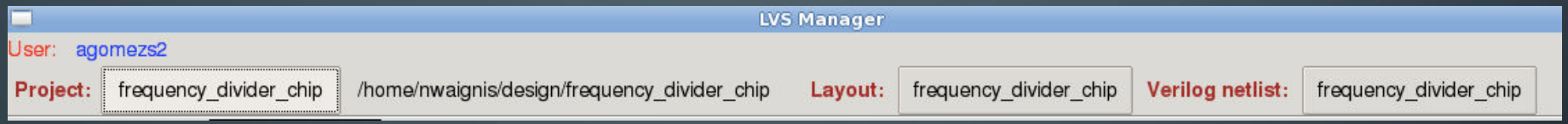
TOP LVL INTEGRATION: ROUTING

- Connect pins to pads
- Connect power busses to pads
- Add global substrate contact
- Add antenna diodes to digital outputs



TOP LVL INTEGRATION: LVS

- Verify Top-level connectivity




```
.subckt frequency_divider vdd gnd in N<0> N<1> N<2> N<3> N<4> N<5> reset out w_n
1073741817_n1073741817#
+ vdd
XDFFQX4_5 BUX2_7/Q vdd gnd NA22X0_3/Q INX0_9/A DFFQX4
XEN2X1_2 gnd vdd NO2X1_5/B EN2X1_2/Q EN2X1_2/A EN2X1
XNA22X0_3 gnd vdd NA22X0_3/Q BUX2_4/Q ON21X0_7/Q NA2X0_17/Q NA22X0
XDECAP3_0_1_0 vdd gnd DECAP3
XON21X0_7 gnd vdd ON21X0_7/Q NA2X0_18/Q AND5X4_1/Q INX0_9/Q ON21X0
XNA2X0_18 gnd vdd NA2X0_18/Q NO2X2_3/A AND3X1_1/Q NA2X0
XNA2X0_15 gnd vdd NA2X0_16/B ON21X1_2/Q N<3> NA2X0
XNA2X0_16 gnd vdd DFFQX4_4/D NA22X0_2/Q NA2X0_16/B NA2X0
XDFFQX4_4 BUX2_7/Q vdd gnd DFFQX4_4/D INX0_8/A DFFQX4
XNO2I1X2_2 gnd vdd NA3X0_8/C NO3X4_2/A INX0_8/A NO2I1X2
XEN2X1_4 gnd vdd NO3X4_2/C EN2X1_4/Q NO3X4_2/A EN2X1
XAO31X1_1 gnd vdd NA3X0_8/A N<1> NA3X0_8/C EN2X1_4/Q AO31X1_1/Q AO31X1
XDECAP3_0_0_0 vdd gnd DECAP3
XMU2IX1_4 vdd gnd NO3X4_2/C AO31X1_1/Q MU2IX1_4/Q NO2X2_3/A MU2IX1
XDFFQX4_2 BUX2_6/Q vdd gnd MU2IX1_5/Q NO3X4_2/C DFFQX4
XMU2IX1_5 vdd gnd INX0_7/Q MU2IX1_4/Q MU2IX1_5/Q BUX2_2/Q MU2IX1
XINX0_7 gnd vdd N<1> INX0_7/Q INX0
XDFFQX4_6 BUX2_7/Q vdd gnd AO32X1_4/Q INX0_10/A DFFQX4
```

```
`include "/home/nwaignis/design/P_frequency_divider/verilog/P_frequency_divider/
frequency_divider.vgl"

module frequency_divider_chip(
  input real VDD3V3,
  input real VDD1V8,
  input real GND,
  input in,
  input [5:0] N,
  input reset,
  output out
);

wire real VDD3V3;
wire real VDD1V8;
wire real GND;
```

SUMMARY

- Full backend and integration flow for a small RTL design in Efabless platform
- No cost, available to everyone
- Streamlined process steps. It took less than 3h (!)
  - Physical Implementation ~ 1h
  - Top level integration ~ 2h
- IP catalog available to provide auxiliary block for your design > Rapid prototyping of new IP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Q & A