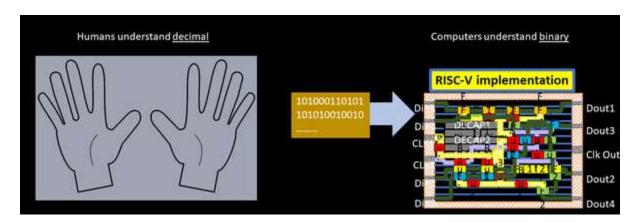


RISC-V doubleword

Let's analyze numbers

Kunal Ghosh



"Statistics and numbers are no good unless you have good people to analyze and then interpret their meaning and importance" – Brendan Rodgers
Hi

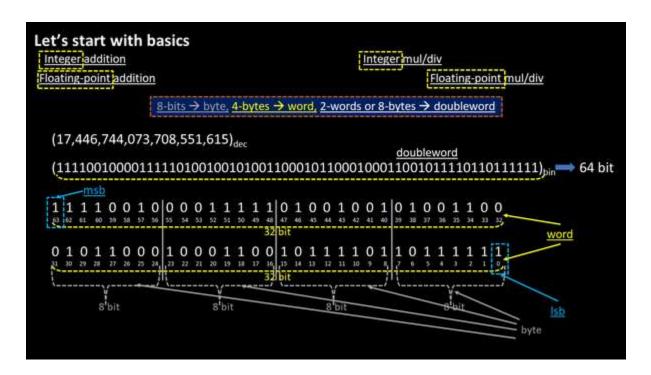
While you all are eagerly waiting for my online course on RISC-V ISA, let's get some basic facts about numbers here – Details will be covered in the course. Stay tuned in below link:

https://www.udemy.com/user/anagha/

• 8-bytes form doubleword

If we break it to a decent level, as shown in below image, it would be a crystal-clear fact for us. I have seen people getting very confused with this one, and so a breakup of the entire doubleword and reconstructing it again, will be very helpful.

Simple and easy - 8-bits form a byte, 4-bytes form a word, 8-bytes form a doubleword. If it's difficult to remember the text, download the below image as reference, and I promise you will never forget it



• RV64 architecture can represent 18,446,744,073,709,551,615 patterns...

...which is from 0 to 2^{64} . That's because RISC-V doubleword is 64 bits long, as shown in above image. In other words, just as a 2-bit can be used to represent numbers 0-3 (i.e. from 0 to $[2^2-1]$), similarly as 64-bit doubleword can be used to represent numbers from 0 to $[2^{64}-1]$. Try evaluating it for 4-bit or 5-bit system

```
Let's start with basics
 Integer addition
                                                                         Integer mul/div
Floating-point addition
                                                                                        Floating-point mul/div
                           8-bits → byte, 4-bytes → word, 2-words or 8-bytes → doubleword
   (17,446,744,073,708,551,615)<sub>dec</sub>
   3 bit
                                                                                                         4 bit
              2 bit
                                                                                                 (0000)<sub>bin</sub>
                                                           (000)hin
                                                                                                              (1000) hin
              (00)<sub>bin</sub>
                                                           (001)_{bin}
                                                                                                 (0001)bin
                                                                                                              (1001)<sub>bin</sub>
              (01)bin
                                                           (010)bin
                                                                                                 (0010)<sub>bin</sub>
                                                                                                              (1010)<sub>bin</sub>
              (10)bin
                                                           (011)<sub>bin</sub>
                                                                                                 (0011)<sub>bin</sub>
                                                                                                              (1011)<sub>bin</sub>
              (11)
                                                                                                              1100)<sub>bin</sub>
                                    Total number of patterns represented by RV64: 264
                                                                                                               1101)<sub>bin</sub>
                                                    i.e. from '0' to '(264 - 1)'
                                                                                                              1110)<sub>bin</sub>
                                                           (111)<sub>his</sub>
                                                                                                 (0111)<sub>bin</sub>
                                                                                                              (1111)<sub>bin</sub>
                                                                                          Total number of Patterns: 25: 16
 Total number of Patterns: 22: 4
                                              Total number of Patterns: 25: 8
     '0' to '(22-1)' i.e. 0 to 3
                                                  '0' to '(23-1)' i.e. 0 to 7
                                                                                               '0' to '(24-1)' i.e. 0 to 15
```

• Positive – MSB is '0', negative – MSB is '1'

This one's easy, as represented in below image, and needed to have an extremely simple hardware. This bit i.e. MSB, is called as sign bit. The method to represent the negative numbers, way to convert negative numbers to its equivalent decimal number, range of positive and negative numbers being represented by RISC-V doubleword, and many such queries will be very well covered in the course.

Range of signed numbers represented by RV64 architecture

This one's is tricky, and needs you understand 1's complement and 2's complement concept (which, by the way, will also be covered). To give you some numbers here, RV64 can represent positive numbers from 0 to $[2^{63} - 1]$ and negative numbers from -1 to -2⁶³ as shown in below image:

Why am I giving you all this information? So that you get prepared, you get excited, you get overwhelmed by what is coming as an online course, which you must have not seen before or expected to be coming.

Learning these courses will give you an additional confident that, be it in any field, if you got strong basics, nothing can move you. If you start from first principle, you can learn any field and become an expert – *To your surprise, the person who's mentoring me on making of VLSI courses is 1974 pass out Mechanical Engineer from IIT Bombay.*

See...I told you.... you got to get your 'first principle' right. Stay tuned to my courses and finish all of them ASAP.